Validation of a State Composer Algorithm for a Cascaded Multicell Converter via Real-Time Simulation

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***Abstract*—The State Composer Algorithm enables a Level-Shifted PWM Modulator to achieve an equal power distribution among the cells of a Cascaded Multicell converter (or similar). This paper reports the implementation and validation of a LS-PWM modulator based on a State Composer Algorithm for a Medium Frequency Railway Traction Converter, supporting up to 10 cells. The results were obtained using a Real Time Simulator.**

***Index Terms*—LS-PWM, Even Power Distribution, Medium Frequency Traction, State Composer Algorithm.**

I. Introduction

Over the last decades, new AC/DC converter topologies for railway traction have been presented [1]–[6]. Based on multilevel arrangements for the input-side and an intermediate DC/DC conversion stage operating in the kHz range [7]–[9], these new topologies aim to eliminate the heavy and bulky line-frequency transformer used in the state-of-the-art railway traction converters. They are usually denominated Power Electronics Transformer (PET) or Medium Frequency Transformer (MFT).

The most prosperous PET topology to date is shown in Fig. 1.a). The prototype published in [8] uses $N = 9$ cells for a 15 kV application (including one cell for redundancy). The intermediate dc-link is rated at 3.6 kV and the output voltage has an equivalent switching frequency at approx. 5 kHz. Thanks to the medium-frequency transformers, the input-side of the PET can be modelled as a classical Cascaded Multicell Converter, as shown in Fig. 1.b).

Due to the large amount of series connected modules (in a single phase), the modulation of the series-connected 4QCs presents challenges and opportunities. The straight-forward modulation alternative for Cascaded-Multicell-type (CM) topologies is Phase-Shifted PWM (as described in [10]), since the technique is well-known and leads to an even distribution of the processed power among the converter's cells. If the carriers are carefully distributed (assigned) among the modules, the harmonic content of some of the common-mode

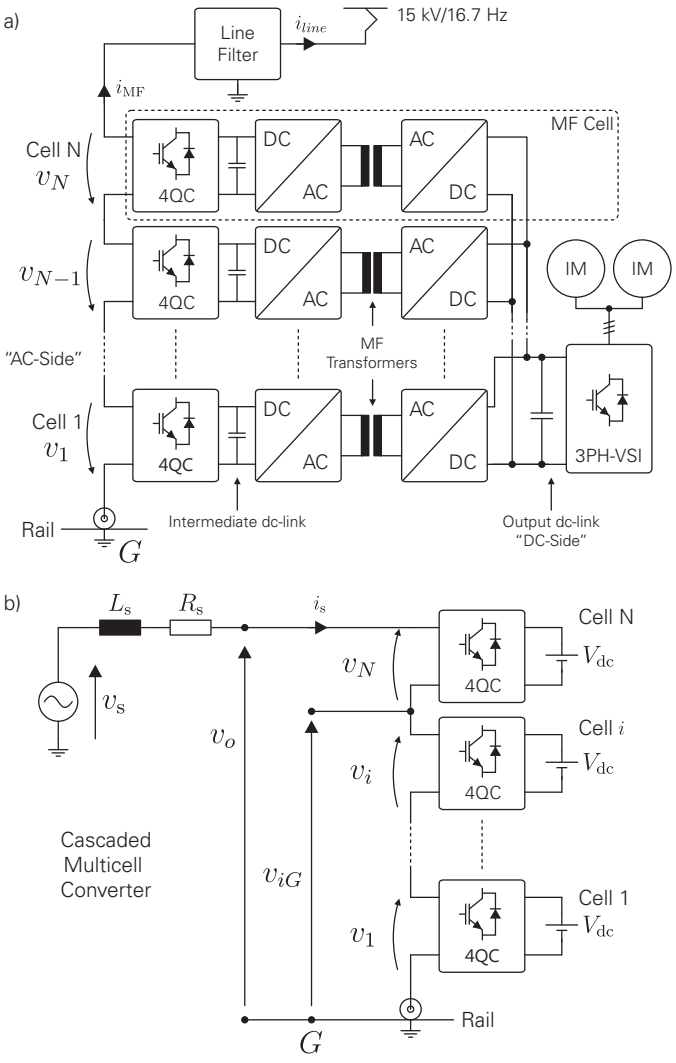

Fig. 1. a) Generalized topology of a medium frequency AC/DC railway traction converter. The converter has N modules connected in series on the AC-side side and parallel connected on the DC-side. b) Equivalent circuit-model for the AC-side of the MF traction converter.

voltages (v_{iG} in Fig. 1.b)) can be improved [11], thus reducing stress on the insulation.

An interesting alternative technique for MF traction converters is Level-Shifted PWM [12]. The technique achieves a similar THD as PS-PWM [13] and its spectrum's characteristics may prove beneficial when designing the line-filter. Unfortunately, the classical LS-PWM implementation distributes the power unevenly among the cells, which is a no-go criteria for railway traction applications.

The State Composer Algorithm (SCA, presented in detail in [14]) produces a LS-PWM voltage pattern for a CM-type converter while ensuring even power distribution. The SCA does not require to measure the dc-link voltage of the individual cells (natural balancing [15]). In addition, the algorithm features an instantaneous transition into $N-1$ operation when a cell is bypassed, maintaining the overall switching frequency constant. Further, the algorithm also has the ability to reduce the harmonic content of common-mode voltages between the cell's outputs and ground (just as in PS-PWM).

This paper reports the implementation and experimental validation of a LS-PWM modulator based on the State Composer Algorithm for a PET as the one shown in Fig. 1. The modulator was implemented in a state-of-the-art control platform based on a C6000 DSP and a Xilinx FPGA and supports up to 10 cells.

II. The State Composer Algorithm

The State Composer Algorithm takes its name from the fact that the converter's switching state at any given time is *composed* online. Since MF Traction converters today have a significantly large amount of cells (typ. $N=9$), the amount of switching states is too large to utilize offline-calculated state-machines such as in [16] in order to distribute commutations evenly among all the cells. Similarly, the method in [17], which adds a discontinuous signal to each of the $2N$ carriers, would result fairly complex to implement in digital hardware, because all registers would need to be dimensioned to fit the complete modulation range with an acceptable resolution. Further, such method might lead to large FPGA resource consumption.

Other novel methods that manipulate the power distribution and which rely on the measurement of the individual dc-link voltages (e.g. [15], [18]) are, for this particular application, rather unsuitable. The main reasons being the large amount of measurements needed, the respective insulation requirements for interfacing to the control hardware (which is usually a central unit on a different potential) and additional costs.

A block diagram showing the principle of operation of the SCA is depicted in Fig. 2. On the left, a LS-PWM modulator identifies the next converter output voltage $L_{k+1} \in \{0, 1, ..., 2N, 2N+1\}$ to be generated, which

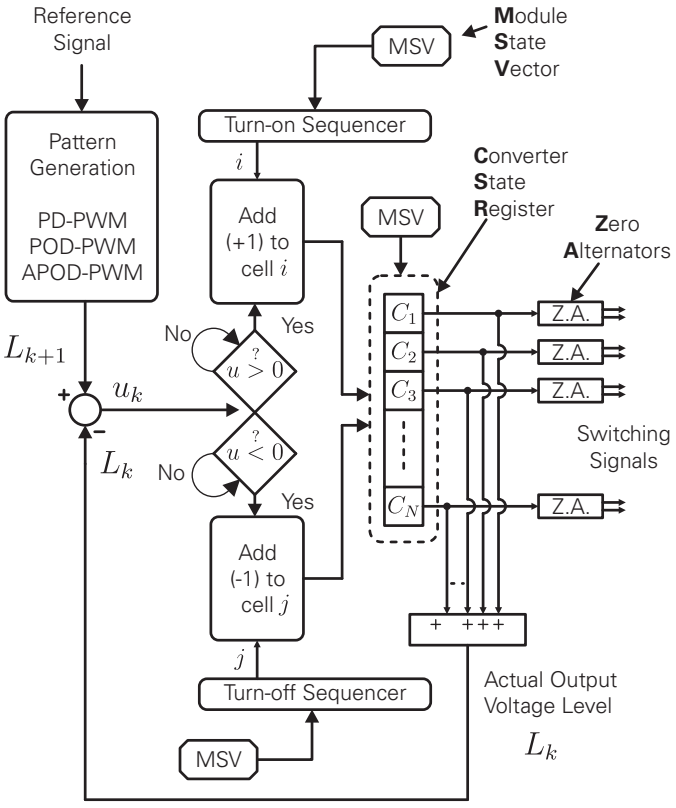

Fig. 2. Block diagram of the principle of operation of the State Composer Algorithm. The output voltage level of the converter is identified utilizing a classical LS-PWM modulator, while the converter's switching state is stored in the Convert State Register (CSR). Due to the redundancy of the zero-voltage output, Zero Alternators make sure to rotate the switching state used for such voltage output.

is in turn the input to the SCA. The SCA's kernel is the State Converter Register (CSR), which holds the actual output-voltage state $C_i \in \{0, 1, 2\}$ of each of the converter's cells ($i = 1, 2, ..., N$). If a cell's output is $-V_{\rm dc}$ ($+V_{\rm dc}$), the CSR's content for that cell is 0 (2). If the cell's output is zero, the CSR is 1. This rather unusual codification helps implement the SCA using positive integers, making the FPGA programming quite simple.

Due to the redundancy of the zero output voltage state in an H-Bridge, Zero Alternators make sure to rotate the switching state used to generate the zero voltage in a given module. Notice that the converter's actual output voltage level is simply $L_k = \sum_{i=1}^{N} C_i$.

As long as $L_{k+1} \neq L_k$, the entries of the CSR are increased (decreased) in unit steps according to a predefined turn-on (turn-off) sequence, thus evenly distributing commutations among the cells. In consequence, it is the carrier frequency f_c what defines the average switching frequency of the 4QCs. For a modulator operating with N cells, the average 4QC switching frequency is $f_{4\rm QC} = f_c/N$. Another effect is that, if the carrier frequency is not modified and one cell is bypassed, then the remaining cells will automatically increase their

switching frequency, thus the apparent converter switching frequency remains constant.

Regarding the turn-on and turn-off sequencers, a careful selection of the sequence allows to reduce the harmonic content of the converter's common-mode voltages (v_{iG} as shown in Fig. 1.b) between the cells' outputs and ground. Ultimately, a Module State Vector (MSV) indicates the sequencers if a cell has been bypassed, so that this cell is discarded from the sequence. Accordingly, the MSV sets the content's of the bypassed cell's entry to one.

III. Modulator Implementation

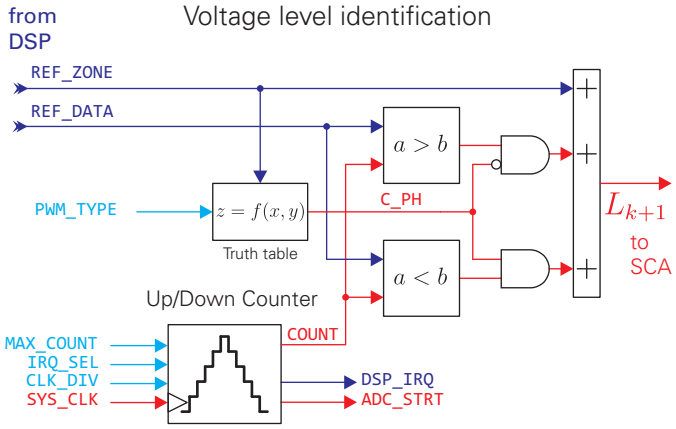

Fig. 3. Block diagram of voltage-level-identification stage in the FPGA for the implemented modulator based on the State Composer Algorithm. A single up/down counter suffices to generate the LS-PWM pattern. The counter is also utilized to interrupt the DSP and initiate ADC conversions. The configuration signal `PWM_TYPE` is used to define the desired PWM pattern (PD, POD or APOD). The signals `REF_DATA` and `REF_ZONE` are calculated in the DSP.

In order to validate the SCA concept, a modulator for LS-PWM patterns supporting up to 10 cells was implemented in a State of the Art digital control platform. In order to minimize resource usage within the FPGA, some minor pre-processing of the modulating signal was realized in the DSP, which allowed to implement the pattern-generation part with a single carrier. A block diagram of the actual implementation is shown in Fig. 3. Notice that the modulator outputs 3 signals for each 4QC: two switching signals (the complementary commands shall be generated locally, for example, by the Gate Drive Unit or GDU) and a 4QC-Enable signal, which allows to indicate that all semiconductors of the module shall be turned off.

The reference signal $r(k)$ is broken down into two components: `REF_DATA` and `REF_ZONE`. The signal `REF_ZONE` indicates the band where the reference is located, while signal `REF_DATA` is the difference between $r(k)$ and the corresponding carrier's minimum value. The bands are numerated in such a way, that the lowermost band in the

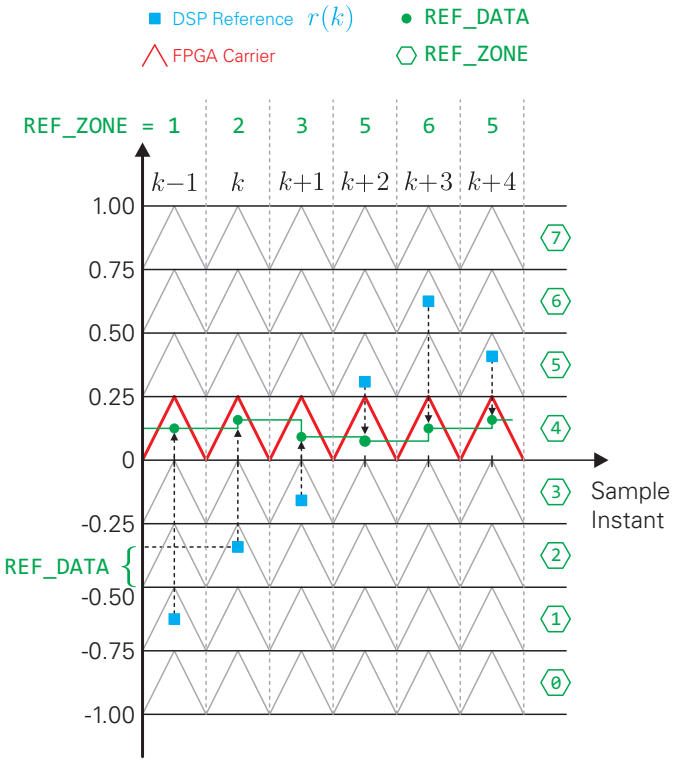

Fig. 4. Example with $N = 4$ for the decomposition of $r(k)$ into `REF_DATA` and `REF_ZONE`.

modulation range is defined as `REF_ZONE=0` and the topmost band is `REF_ZONE`$=2N-1$. An example for $N = 4$ is shown in Fig. 4 for symmetrically sampled PD-PWM, where it can be easily recognized that this process is equivalent to the projection of the reference signal into the carrier directly above zero.

Once in the FPGA, the value in `REF_DATA` is compared against the carrier (signal `COUNT` in Fig. 3) implemented using an up/down counter of appropriate resolution, with two different polarities, which enables the implementation of the PD, POD and APOD patterns. Depending on signal `C_PH` (Carrier Phase), the result of either `REF_DATA` > `COUNT` or alternatively `REF_DATA` < `COUNT` is added to `REF_ZONE`, resulting in signal L_{k+1} with the desired LS-PWM variant. Notice that $a < b$ is equivalent to $a > -b$ as long as both a and b are positive, which is always the case in the FPGA.

The SCA as such is relatively simple to implement and will not be further detailed. The complete algorithm (since L_{k+1} changes until the switching signals are updated) requires 7 clock cycles to execute (the FPGA's clock operates at 100 MHz, ergo the algorithm requires 70 ns) and during this period of time variations of L_{k+1} are ignored.

IV. Test Bench Setup

In order to verify that the implemented modulator operates according to specification, a test-bench based on a Real-Time Simulator (RTS) was utilized. The setup is depicted in Fig. 5.

The RTS is based on dSpace hardware and is meant to emulate the converter of Fig. 1.a) with an integration step-size of $T_{\mathrm{RTS}} = 25\,\mu$s. As published in [10], the control of the PET requires to measure only the line-voltage, line-current and the secondary-side dc-link voltages, ergo only three analog signals are going from the RTS towards the control platform. The signal conditioning device adapts the outputs of the RTS to the particular control hardware.

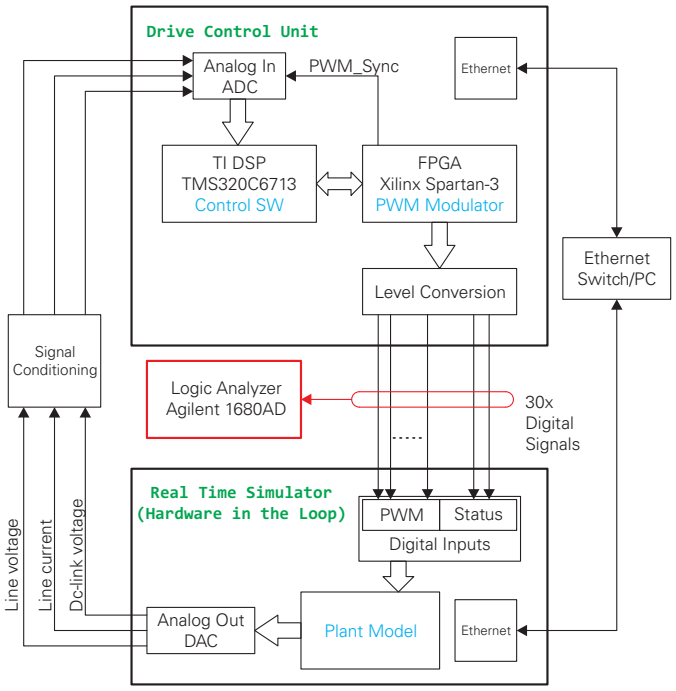

Fig. 5. Block diagram of the test-bench setup used for the modulator validation. A dSpace HIL is used to emulate the target hardware and an Agilent logic analyzer is utilized to record the digital signals from the FPGA.

On the other edge of the RTS, 30 digital inputs accommodate the modulator's outputs. For each converter cell, two switching signals (PWM) plus an enable (Status) are considered. Since the RTS cannot react asynchronously to changes in the switching signals in real time, the PWM inputs are actually averaged over T_{RTS}, returning a mean on-time for this period. Ethernet interfaces in both control unit and RTS allow the user to access process-data in real time in both devices.

The only external measurement device in the setup is an Agilent 1680AD Logic Analyzer, which is utilized to record the PWM switching signals with a very high time-resolution (200 ns per signal). These measurements allow to reconstruct the PWM voltage patterns and verify that the patterns coincide with the theory.

V. Test Results

A. LS-PWM Pattern Generation

As stated in Section III, the implemented modulator can generate PD, POD and APOD patterns. To verify that the patterns are generated correctly, the switching signals coming from the FPGA are recorded with the logic analyzer. Using Matlab, the recorded data is processed to reconstruct the converter voltage v_o that would be generated by an equivalent converter as the one in Fig. 1.b) with $V_{\mathrm{dc}} = 3600\,\mathrm{V}$. This waveform is then compared against the output of an ideal LS-PWM modulator implemented in Simulink.

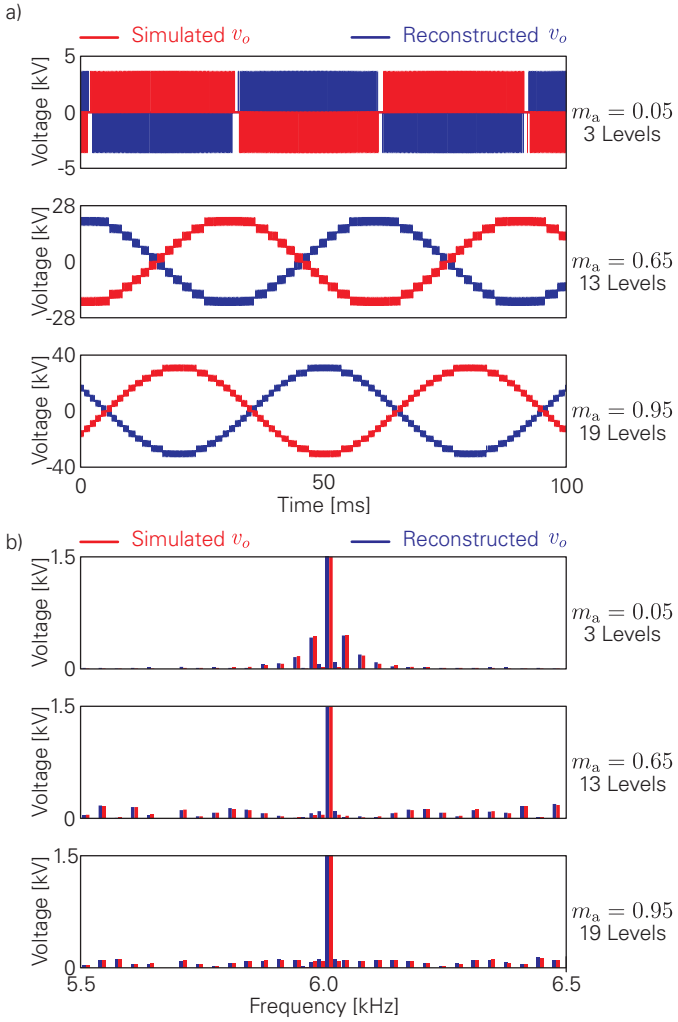

Fig. 6. Test results for the PD-PWM pattern generation. a) Time-domain measurement and ideal voltage waveforms for modulation indexes $m_a \in \{0.05, 0.65, 0.95\}$. b) Spectra around the first carrier harmonic bundle.

The test results for PD-PWM are shown in Fig. 6 for three different modulation indexes. The time-domain waveforms are shown in Fig. 6.a), where the simulated signal has been inverted to simplify the visualization. The time-domain results show identical waveforms, ergo a frequency analysis as shown

in Fig. 6.b) can actually demonstrate that PD-PWM has been achieved without any noticeable errors.

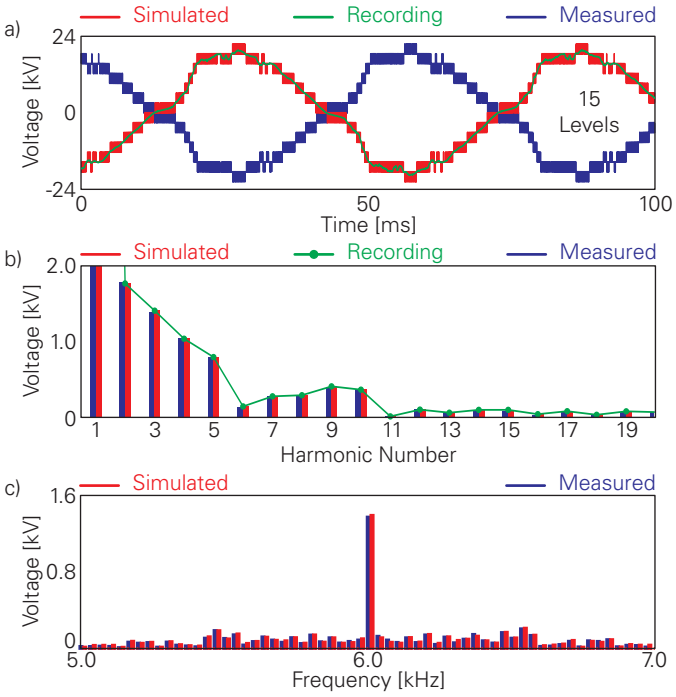

Fig. 7. Test results for the APOD-PWM pattern generation. a) Time-domain signals. b) Spectra for the baseband harmonics. c) Spectra around the first carrier harmonic bundle.

Since the modulator is expected to operate a railway traction converter, the sinusoidal modulating signal has been replaced with a recording from a 15 kV railway supply. In this case, the modulating signal comes from the RTS and is sampled by the control unit. The DSP scales the measurement considering a total AC-side dc-link of $N{\cdot}3600$ V in order to generate the modulator's reference signal. The diagrams of Fig. 7 show a successful implementation even for a harmonic-rich reference signal. The waveforms in Fig. 7.a) do not show any deviations between measured and expected results. The spectra from Fig. 7.b) and Fig. 7.c) confirm very good performance of the modulator. Similar tests were also executed for POD-PWM and APOD-PWM, however they are not included in this paper since they do not provide any additional information with regard to the previous results.

B. On-line Cell Bypass and Common-mode Voltage Improvement

The SCA features a very simple mechanism to transition into operation with a bypassed module. In fact, the algorithm can continue operation with down to one remaining module, however this is only a theoretical case. A further feature, explained in detail in [14], is the capability to improve some of the common-mode voltages of the converter by proper selection of the sequences. These features are validated in this section. In a similar fashion as in Section V-A, the logic analyzer records the generated switching signals and using Matlab the corresponding voltage waveforms are reconstructed.

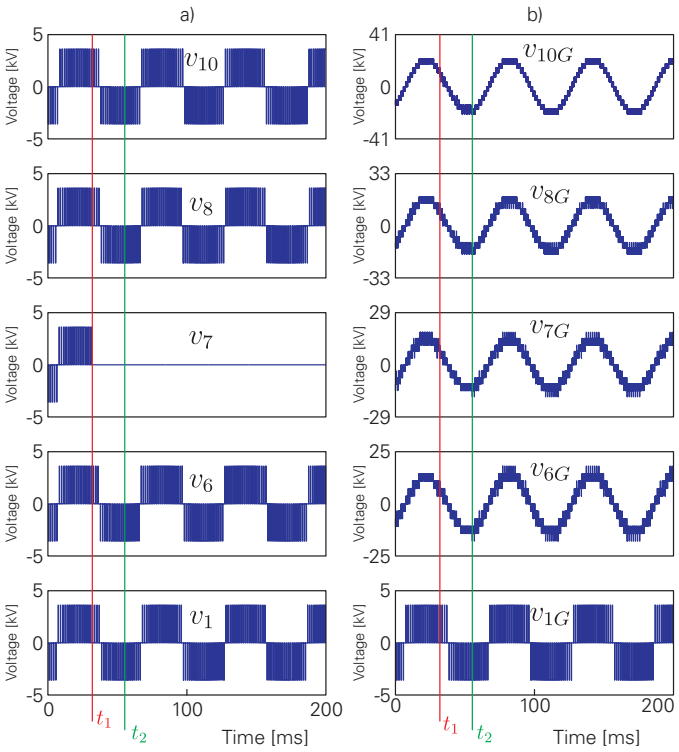

Fig. 8. Test results for single-cell bypass. At instant $t = t_1$ the switching signals of cell 7 are disabled. At instant $t = t_2$ the modulator's MSV is informed to discard the module. a) Output voltages for cell 1, 6, 7, 8 and 10, where it can be seen that the operative cells do not stop operation as the modulator is updated. b) Some of the converter's common-mode voltages. Thanks to the optimized sequence, significant low-frequency switching harmonics are cancelled.

In order to verify both features simultaneously, a single-cell bypass is executed. The test commences with 10 operational cells with a carrier frequency of $f_c = 6012$ Hz. The sequencers are configured with sequence $S = \{C_1, C_5, C_9, C_3, C_7, C_6, C_2, C_{10}, C_4, C_8\}$. At instant $t = t_1$ the switching signals of cell 7 are disabled to simulate a GDU failure. At instant $t = t_2$ the MSV is updated, indicating that cell 7 is to be discarded from the turn-on(off) sequences. The test results, shown in Fig. 8 for cells 1, 6, 7, 8 and 10, demonstrate a successful and seamless transition into $N - 1$ operation. Notice that apart from cell 7, all other modules continue switching as the modulator adjusts the sequences. On the right side of Fig. 8 are shown the common-mode voltages associated to the mentioned cells. Notice that the waveforms do not present the switching harmonics at multiples of f_c/N which would be the case (as already shown in [14]) if the trivial sequence $S = \{C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8, C_9, C_{10}\}$ would be used.

A zoomed view of the results is shown in Fig. 9 around instant $t = t_1$. The voltage waveform for cell 7 shows that

the pulsing of that cell stops at $t = t_1$. As this occurs, the voltage waveform of the converter voltage v_o presents some distortion due to the missing pulses from cell 7, however, as soon as the modulator is reconfigured *on-line*, the distortion disappears. The output voltage of cell 1 (any other cell could have been used) shows that the switching period (or frequency) is slightly reduced (increased, respectively.). The variation is expected, because the carrier frequency has remained constant. In general, the 4QC switching frequency is $f_{4QC} = f_c/N$, where N is the number of *active* modules, ergo before the bypass $f_{4QC} \approx 601.2\,\text{Hz}$ and with $N - 1 = 9$ cells, $f'_{4QC} \approx 668\,\text{Hz}$. These theoretical values coincide (within an acceptable tolerance) with the measured results.

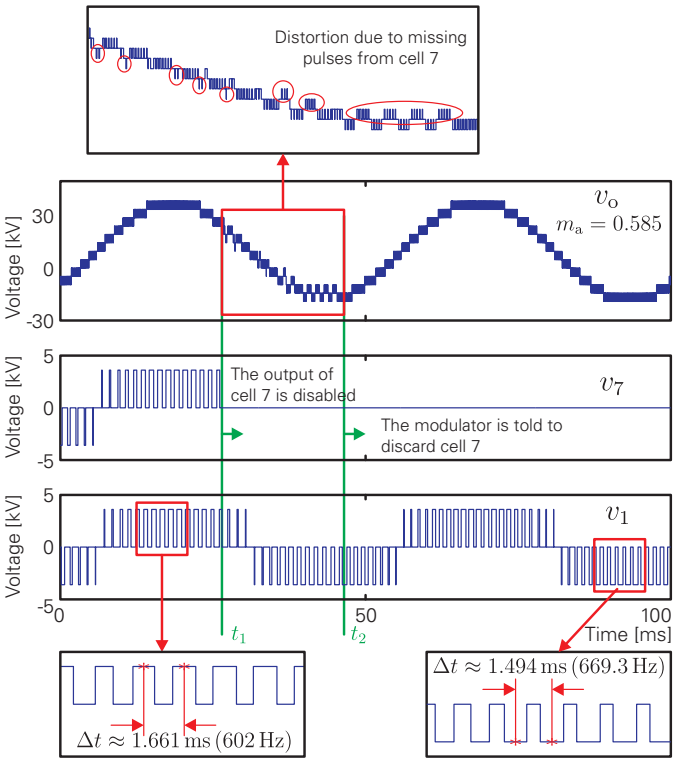

Fig. 9. Test results for single-cell bypass and common mode voltage improvement. Notice that the apparent switching frequency of cell 1 (or any other not-bypassed cell) increases slightly after $t = t_2$, as the carrier frequency remains unchanged.

C. Even Power Distribution

It remains to validate that the power processed by each cell is, in average, equal. One simple alternative to check this would be to analyze the fundamental of each of the cell's voltages. If they are identical in all cells, then all cells process the same power, as they share the same current. This condition is, however, necessary but not sufficient to demonstrate proper operation, as slow transients or sporadically occurring events might not be caught on a fundamental period. In any case, measuring the switching pulses with a high time-resolution for prolonged periods is not possible due to limited memory in the logic analyser.

As an alternative approach, the system in Fig. 10 is utilized. The hypothesis is quite simple: given the input current is controlled (and ergo the converter's input power), then, if each cell processes the same amount of power, then the dc-links will converge to an equal average voltage, as the load resistor R_L is identical in every cell. Further, the dc-links are preloaded to random (and different) voltages around 3 kV in order to emphasise that the dc-links converge regardless of the initial conditions. The system parameters are $R_\text{L} = 129.6\,\Omega$, $C_{\text{p}i} = 600\,\mu\text{F}$, $R_\text{s} = 0.2\,\Omega$ and $L_\text{s} = 35\,\text{mH}$.

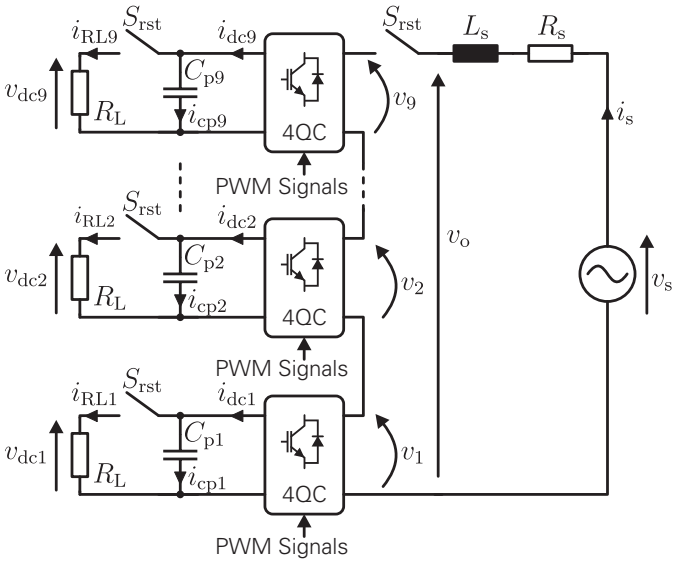

Fig. 10. Circuit of the modelled system for the even power distribution validation. The load resistors and dc-link capacitors are identical in each of the nine cells, however the dc-links are preloaded to random (and different) voltages around 3 kV. The load resistors draw 100 kW if the dc-link is constant at 3600 V.

The most relevant test results are shown in Fig. 11 and Fig. 12. The waveforms of Fig. 11 show an overview of i_s, the converter's PWM-modulated voltage v_o and the nine individual dc-link voltages for the first 400 ms. These waveforms were captured using the user interface (Control Desk) of the RTS, and as a consequence, no signals from the DSP could be recorded.

It results immediately clear that the even power distribution capability of the State Composer Algorithm is achieved successfully, as all dc-link voltages evolve to a mean value of 3.5 kV. Notice that the spikes in v_o are not an error or flaw in the PWM modulator, but are originated by the asynchronous read of the digital inputs in the RTS. This is confirmed by the fact that no such distortions were measured in the waveform generation tests (see Section V-A).

The test was designed so that the dc-links would settle at 3.6 kV, however the measurement shows a 3.5 kV DC level. This is caused by a small phase offset between v_s and i_s, caused by the non-infinite gain of the current controller used.

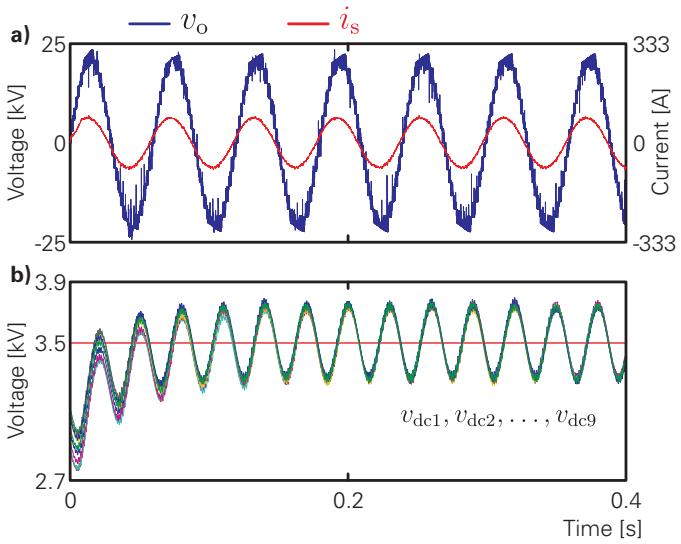

Fig. 11. Relevant waveforms for the even power distribution test for the first 400 ms. a) Converter voltage v_o and line-current i_s. b) Dc-link voltages for cells 1 to 9. All cells converge at an average of 3.5 kV, demonstrating proper even power balancing of the cells.

This error is, however, completely irrelevant and not related to the implemented PWM modulator.

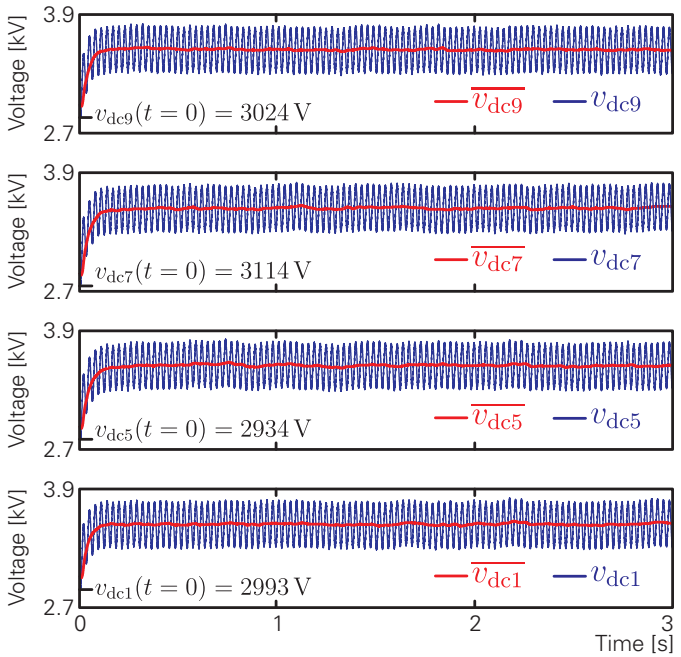

Fig. 12. Dc-link voltages for cells 1, 5, 7 and 9 for a three second period. The measurement demonstrates an stable modulator performance for a prolonged period of time. The time constant for the dc-link voltages is governed by the control dynamics, R_{L} and $C_{\mathrm{p}i}$.

To demonstrate that the dc-link voltages remain balanced during a long period of time, the results of Fig. 12 show the voltage waveforms for cells 1, 5, 7 and 9 for a three second period. Their initial voltages and mean values are also shown, so it is easier to observe how the voltages converge.

VI. Conclusions

The State Composer Algorithm, proposed and theoretically described in [14], has has been experimentally validated using a Real Time Simulator. Although the target application is a Power Electronics Transformer for traction applications, the algorithm can be applied to any single- or three-phase application based on Cascaded Multicell converters.

The test results have demonstrated that the LS-PWM modulator based on the SCA is not only capable of generating near ideal PWM patterns, but also features a seamless transition into $N-1$ operation and harmonic improvement of some of the converter's common-mode voltages.

The implemented modulator features little resource consumption, as the PWM pattern identification is actually realized with a single carrier.

Measurements for final validation with a laboratory prototype in order to account for unmodeled phenomena, such as the effects of interlocking time and non-ideal IGBT commutation, will follow in the near future.

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