Comparison of Press-Pack IGBT at Hard Switching and Clamp Operation for Medium Voltage Converters

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Keywords

<<IGBT>>, <<Device characterization>>, <<Test bench>>, <<Packaging>>, <<Device application>> and << Industrial application >>.

Abstract

The newly developed press-pack IGBT devices compete with IGCTs in high power industrial applications. These new semiconductors were already studied in detail for hard switching [1] and for clamp operation [2]. Nevertheless, a comparison of the basic switching characteristics of the IGBT press-pack devices for hard switching and clamp operation has not been done so far.
This paper compares the switching behavior, the switching losses and the safe operating area trajectories of the new 85 mm, 4.5 kV, 1.2 kA press-pack SPT$^+$ IGBT for hard switching and clamp operation. The methods used for the experimental characterization and comparison are explained in detail.

Introduction

Nowadays medium voltage converters are essential for the application areas industry, traction, marine and energy. They increase the efficiency of processes, allowing better control of the energy flow. Power semiconductors are the basic building block of medium voltage converters, and their development has enabled a substantial improvement of the converter technology during the last years [3–5]. Up to now, IGBT modules and IGCT press pack devices have shared the market of self commutated medium voltage converters. Recent trends suggest that self-commutated converters will be the dominating technology for applications below 30 MVA in the middle term [6, 7].
Press-pack IGBTs combine the advantages of IGBT dies with those of press-pack housing, making them an attractive alternative to IGCTs [8–11]. The static and switching behavior of the new 85 mm, 4.5 kV, 1.2 kA press-pack SPT$^+$ IGBT at hard switching was described in [1]. Reference [2] proposes the use of a clamp circuit for the aforementioned IGBT. An IGBT press pack device offers the potential of a high power cycling capability, an explosion free converter design, and low switching and total losses. Obviously, the IGBT press pack devices have become an interesting alternative to IGCTs in high power medium voltage applications. [8, 10]
This paper presents a detailed comparison of the switching behavior, the switching losses and the semiconductor stress of both modes of operation for diverse collector currents and junction temperatures.

Semiconductor Data and Test Bench

For the comparison of the switching behavior and switching losses of the new 4.5 kV, 1.2 kA press-pack *Soft-Punch-Through Plus* (SPT$^+$) IGBT T1200EB45E four configurations have been tested:

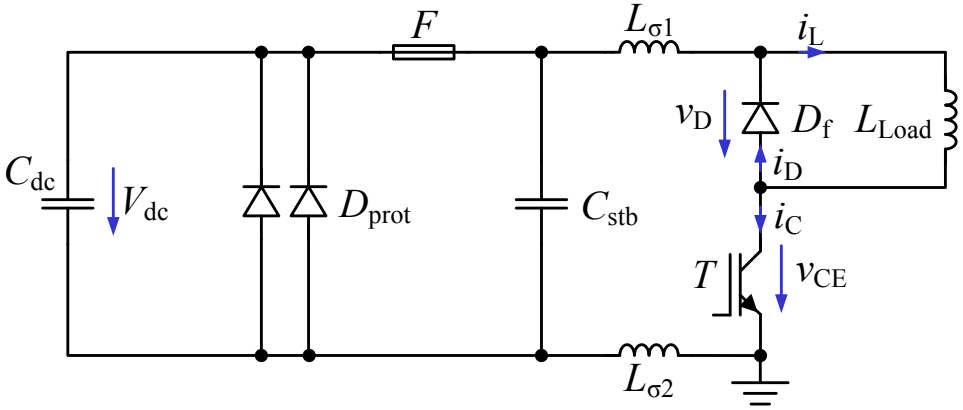
- Hard Switching with a stray inductance of 120 nH
- Clamp 1 with $L_{\text{cl-1}} = 1\,\mu\text{H}$
- Clamp 2 with $L_{\text{cl-2}} = 2\,\mu\text{H}$
- Clamp 3 with $L_{\text{cl-3}} = 5.6\,\mu\text{H}$

Table I: Semiconductor data

Device	Diode	IGBT
Manufacturer	Infineon	Westcode
Model	D 1031SH	T1200EB45E
Diameter	62.8 mm	85 mm
Si-area	3097 mm^2	4284 mm^2
Active Si-area A_{aSi}	2463 mm^2	2142 mm^2
R_{thJH} (2 sides)	14.1 K/kW	9 K/kW

Table II: Semiconductor core values

Diode		IGBT	
V_{RRM}	4500 V	V_{CES}	4500 V
I_{FRMSM}	2300 A	$V_{DC\text{-}link}$	2800 V
I_{FAVM}	1470 A	$I_{C(DC)}$	2132 A
I_{RM}	1500 A	$I_{C(nom)}$	1200 A



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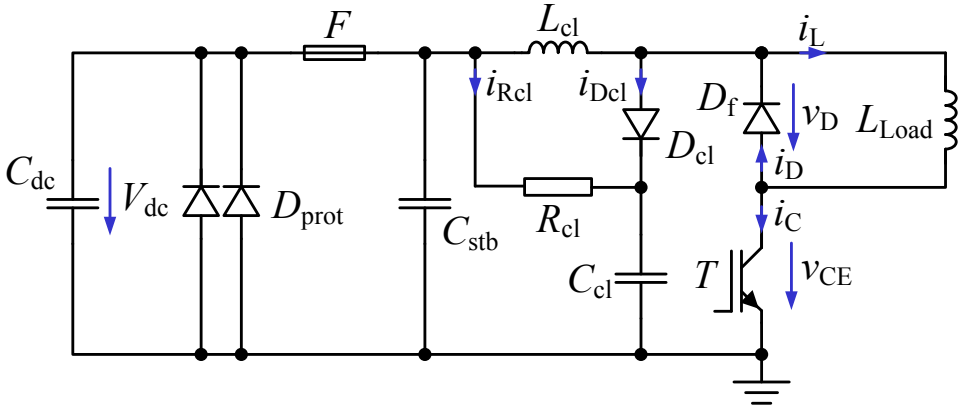


(b)

Figure 1: Test bench schematic diagram for (a) hard switching and for (b) soft switching with clamp circuit

The test setup includes the diode D1031SH as freewheeling diode D_f as well as clamp diode D_{cl}, and the commercially available gate unit C0030BG400 ($R_{G,on} = 3.3\,\Omega$ and $R_{G,off} = 2.2\,\Omega$). The semiconductor data are summarized in Tables I and II. The test bench schematic diagram for the different operation modes is shown in Fig. 1. The clamp circuit design is detailed in Table III.
The test circuit is a buck converter, which allows the study of the switching behavior of an active switch (e.g. IGBT, IGCT) and its corresponding freewheeling diode through the use of a double-pulse switching pattern [3]. The dc-link was buffered near to the stack by an extra capacitor C_{stb} (220 µF) in order to

Table III: Test bench and current snubber setup

Test bench		Clamp circuit	
C_{dc}	4.5 mF	C_{cl}	10 µF
C_{stb}	220 µF	R_{cl}	0.5 Ω
L_{Load}	1 mH	L_{cl}	1, 2, 5.6 µH
V_{dc}	2.5 kV		

(a) (b)

Figure 2: Experimental setup (a) IGBT stack for hard switching, (b) stack with clamp circuit

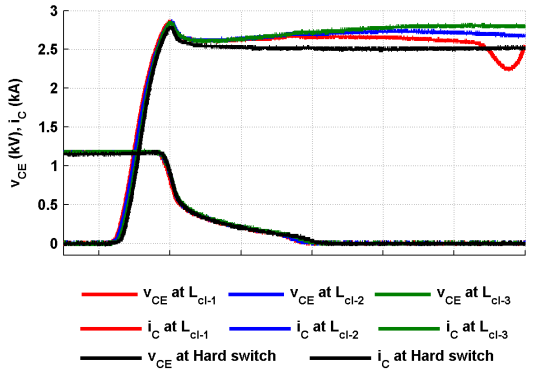
achieve a low stray inductance.
A robust mechanical design was accomplished using 2 mm-thick copper plates connecting the dc-link capacitor C_{dc}, the additional buffer capacitor C_{stb} and the stack. Thus, the mechanical construction of the test bench is able to withstand short circuit currents of about 200 kA in case of a device failure. The two diodes D_{prot} limit possible negative voltages across the dc-link capacitor, preventing an oscillation of the short circuit current and the fuse F avoids the complete discharge of the dc-link capacitors through the stack in failure case limiting the maximum short circuit current to value of less than 60 kA. These are two important components of the safety concept of the test bench.
The junction temperatures of the devices are adjusted by two ring heaters mounted in the stack, controlling the case temperature [3]. The dc-link capacitor is charged by a high-voltage power supply before the measurements are carried out. A partially automated measurement system was used. The values of V_{dc} and I_L are set using a LabVIEW program on a PC connected to the test bench by optical fiber cables. The measurements are captured by two 8 bit four-channel digital oscilloscopes (Tektronix TDS714L), capable of working at a 500 MS/s sample rate. The storage and analysis of the data is carried out on an extra computer. The experimental setup is shown in Fig. 2.

Comparison of 4.5 kV, 1.2 kA Press-Pack IGBT at Hard Switching and Clamp Operation

The press-pack IGBT was characterized for hard switching and clamp operation for different gate resistances R_G, collector currents i_C, dc-link voltages V_{dc} and junction temperatures T_j, as Table IV shows. Hard switching and clamp operation are compared regarding the stress in the safe operating area (SOA), peak power, semiconductor switching losses and clamp switching losses. The definitions of the quantities used for the calculations (e.g. di/dt, dv/dt) correspond with those presented in [1, 2].

Comparison of SOA Trajectories and Maximum Instantaneous Power

The press-pack IGBT and the freewheeling diode feature a smooth switching behavior in all investigated operating points. Waveforms of device voltages, currents and instantaneous power as well as SOA tra-



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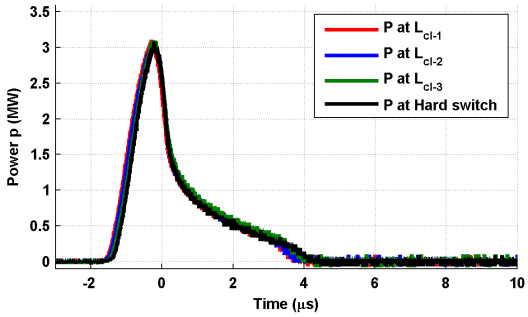

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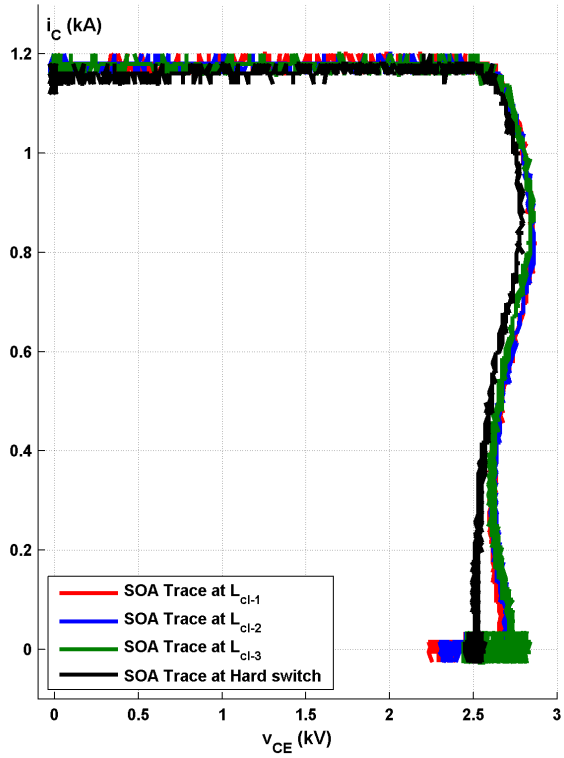
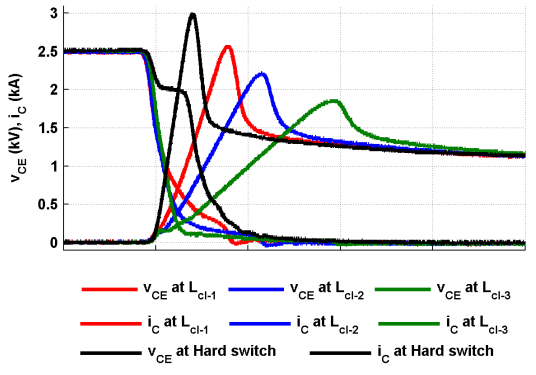


(c)

Figure 3: IGBT turn-off behavior (a) waveforms, (b) peak power, (c) Safe Operating Area trajectories ($T_j = 125\,°C$, $V_{DC} = 2.5\,kV$ and $i_C = 1.2\,kA$)



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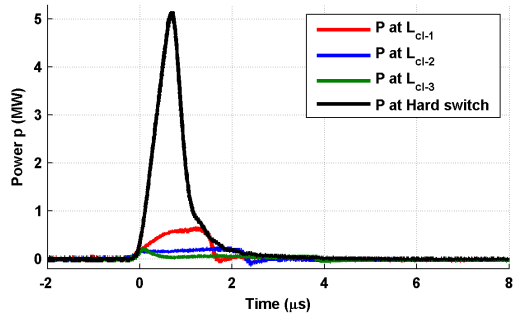

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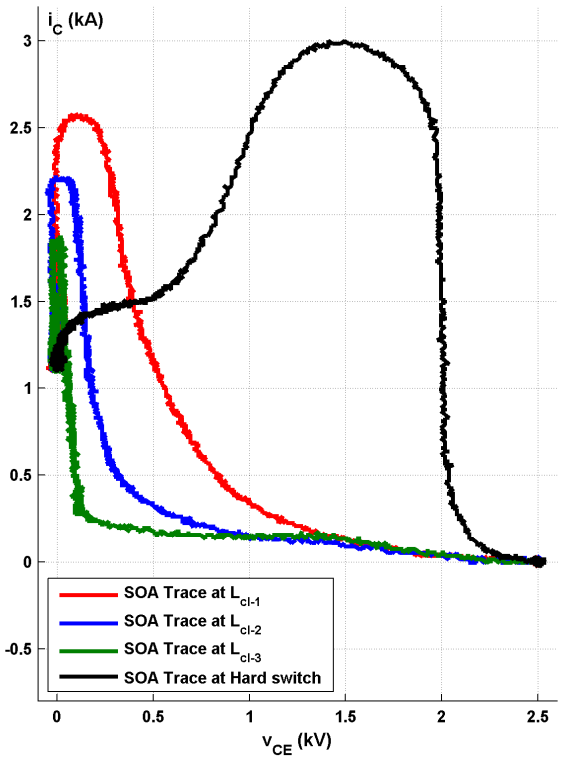

(c)

Figure 4: IGBT turn-on behavior (a) waveforms, (b) peak power, (c) Safe Operating Area trajectories ($T_j = 125\,°C$, $V_{DC} = 2.5\,kV$ and $i_C = 1.2\,kA$)

Table IV: Conducted measurements

Hard Switching	
Variable	Value
V_{dc}	2000 and 2500 V
i_L	100, 300, 600, 900, 1200, 1500 and 1800 A
T_j	25, 60, 90, 125 °C
L_σ	120 and 210 nH
$R_{G,on\text{-}1\ldots3}$	3.3, 5.6 and 6.8 Ω
$R_{G,off\text{-}1\ldots3}$	2.2, 3.6 and 6.8 Ω
Clamp Operation	
Variable	Value
V_{dc}	2000 and 2500 V
i_L	100, 300, 600, 900, 1200, 1500 and 1800 A
T_j	25, 60, 90, 125 °C
$L_{cl1,2,3}$	1.0, 2.0 and 5.6 µH

jectories at $V_{dc} = 2.5$ kV, $i_C = 1.2$ kA, $T_j = 125$ °C and the lowest recommended gate resistance illustrate the behavior of the semiconductors for the selected hard switching and clamp operation (Figs. 3 to 5).
The turn-off behavior of the IGBT is almost not influenced by the different clamp configurations, confirming the adequate selection of the clamp components. The clamp inductance L_{cl} induces a small overvoltage caused by the demagnetization (Fig. 3a), which does not affect the peak power (Fig. 3b), but slightly increases the turn-off losses by about 8 % compared to hard switching.
The clamp inductance has a remarkable influence on the turn-on transient, changing the di_C/dt from 4.2 kA/µs for GU-1 ($R_{G,on\text{-}1} = 3.3\,\Omega$ and $R_{G,on\text{-}1} = 2.2\,\Omega$) at hard switching to 0.5 kA/µs for operation with $L_{cl\text{-}3}$, keeping dv_{CE}/dt at roughly 3.5 kV/µs (Fig. 4a). Moreover, the clamp reduces the turn-on stress of the IGBT in contrast to hard switching: the collector current i_C rises with a low device voltage, which reduces the IGBT turn-on peak power by approximately 95 % from 5.15 MW for hard switching to 0.23 MW for $L_{cl\text{-}3} = 5.6$ µH (Fig. 4b). The turn-on SOA traces of the clamp-operated IGBTs show a substantially larger distance to the SOA margins than the IGBT at hard switching (Fig. 4c). Obviously, the maximum collector current i_C at IGBT turn-on is smaller for IGBTs at clamp operation, due to the reduction of di_C/dt, which also affects the reverse-recovery behavior and losses of the corresponding freewheeling diode.
As expected for the diode, the reverse recovery current is reduced as the clamp inductance L_{cl} is increased, see Fig. 5a (a lower di_D/dt reduces the reverse recovery charge). Accordingly, the diode presents the highest stress for the operation with clamp 1 ($L_{cl\text{-}1}$), caused by the larger voltage peak generated through the combination of a still considerable di_D/dt and the relatively large stray inductance of the clamp circuit configuration (Fig. 5b). An increase of L_{cl} reduces the di_D/dt, the peak reverse recovery current and the rate of current change of the decrease of the reverse recovery current. Thus, the instantaneous peak power decreases for $L_{cl\text{-}2}$ and $L_{cl\text{-}3}$.
The diode turn-off SOA traces show that the hard switching operation approaches to the i_D margins of the SOA, whereas the clamp operation increases the distance to this limit, but reduces the distance to the diode voltage v_D limit (Fig. 5c). The diode presents maximum stress at turn-off transients; the clamp configuration can reduce or increase this stress depending on the relation between clamp inductance, stray inductance, peak reverse recovery current and rate of change of the decrease of the reverse recovery current. A poor design can generate large diode voltage peaks, increasing the stress of the diode.
For the studied operating points, the press-pack IGBT is subject to the largest stress at hard switching during turn-on, and with clamp operation during turn-off transients. The maximum stress is reduced by about 40 % compared to hard switching, due to the addition of a clamp circuit.

Comparison of Losses

The main goal of the use of the clamp configuration is the reduction of the IGBT switching losses. Of course also the diode losses and the total converter losses should not increase compared to hard switching. The semiconductor switching losses of IGBT and diode ($E_{sw,SC}$) are defined as:

$$E_{sw,SC} = E_{on,IGBT} + E_{off,IGBT} + E_{off,Diode} \tag{1}$$

with

$E_{on,IGBT}$: IGBT turn-on switching losses

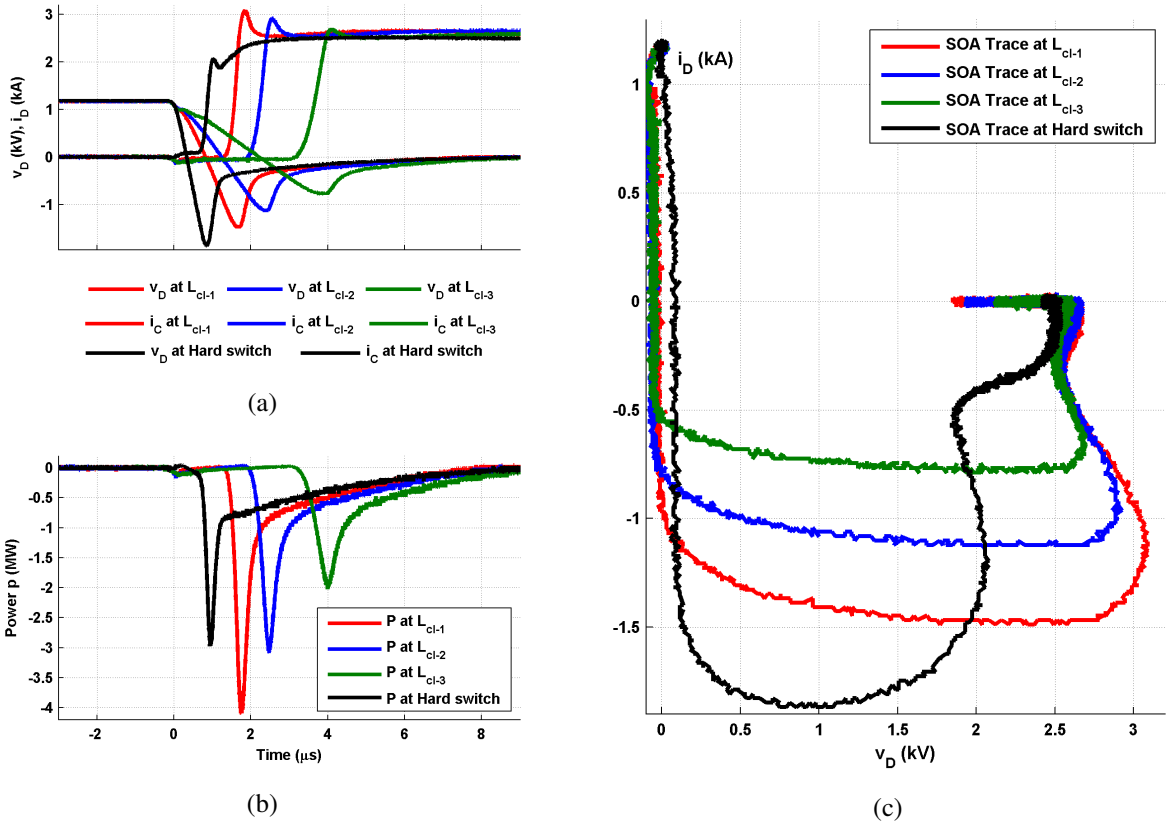

Figure 5: Diode turn-off behavior (a) waveforms, (b) peak power, (c) Safe Operating Area trajectories ($T_j = 125\,°C$, $V_{DC} = 2.5\,kV$ and $i_C = 1.2\,kA$)

$E_{off,IGBT}$: IGBT turn-off switching losses

$E_{off,Diode}$: Diode turn-off switching losses

In case of clamp operation, the clamp and semiconductor losses caused by switching transients are calculated by (2), which includes the additional losses of the clamp diode $E_{D,cl}$ and clamp resistor $E_{R,cl}$. Stationary losses of the clamp inductor (caused by the parasitic ohmic resistance) and the clamp capacitor (caused by the equivalent parallel resistance) are neglected.

$$E_{sw,SC+cl} = E_{sw,SC} + E_{D,cl} + E_{R,cl} \tag{2}$$

The semiconductor and clamp switching losses of the four selected configurations were compared at $V_{dc} = 2.5\,kV$, $T_j = 125\,°C$ and $i_C = 600$ and $1200\,A$. The results can be seen in Fig. 6. The values on top of the columns are the semiconductor and clamp switching losses ($E_{sw,SC+cl}$) and the values in parentheses are the semiconductor switching losses.
The semiconductor switching losses were reduced by 13 to 30 % (clamp 1 to 3 respectively) for clamp operation compared to hard switching. The largest loss reduction by the clamp circuit was achieved during IGBT turn-on. However, the sum of the semiconductor and clamp switching losses were reduced by less than 3 % at 600 A and less than 11 % at 1200 A , which means that a major part of the turn-on losses are transferred from the IGBT to the clamp resistance R_{cl}.
The larger reduction of the semiconductor switching losses is achieved by $L_{cl\text{-}3}$. However, the selection of a clamp should consider the stress of the semiconductors, both switching and clamp losses and particular specifications for the application (e.g. dv/dt, power density, reliability, mounting cost, etc.).
For example, in the studied cases, clamp 2 presents a good trade off between a reduction of semiconductor switching losses, clamp switching losses and stress of the diode. The diode stress is increased marginally (3.37 %), achieving a reduction of the semiconductor switching losses of 25 % and a reduction of the semiconductor and clamp switching losses of 8 %. This allows the reduction of the cooling system or a higher converter output power. However, finally an optimum for criteria like volume, weight, efficiency and costs must be found. The realization of a clamp seems to be an interesting option.

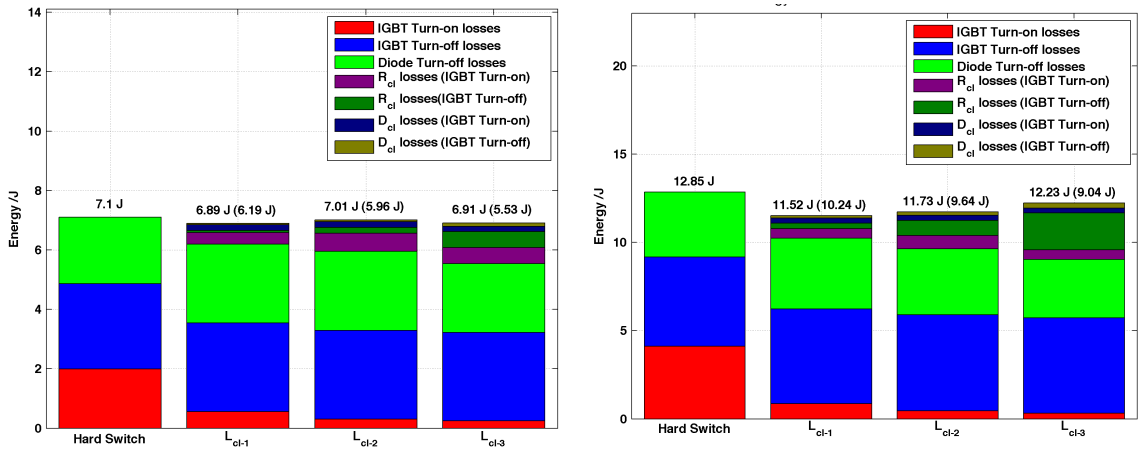

Figure 6: Semiconductor and clamp switching losses ($V_{dc} = 2.5\,kV$, $T_j = 125\,°C$, $i_C = 600\,A$)

Conclusions

This paper shows a detailed comparison of the switching behavior and switching losses of the press-pack IGBT T1200EB45E at hard switching and clamp operation. It shows that the use of clamp circuits for press-pack IGBTs features interesting characteristics like reduced switching losses (up to 30 %) and less stress of the semiconductors (lower di_C/dt, reverse recovery current and peak power for IGBT and diode). The optimum clamp circuit will depend on the specification requirements of the particular application. The saved semiconductor switching losses enable an increase of the converter power or switching frequency in medium voltage converters, since both characteristics are limited thermally by the semiconductor losses and the cooling configuration. It is remarkable that the sum of switching and clamp losses are lower than at hard switching. For example the sum of switching and clamp losses are reduced by about 3 % at 50 % and 11 % at 100 % rated current.

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