Design and Losses of PWM Current Source Converters

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***Abstract*—The aim of this paper is to present a complete design procedure for a current source converter (CSC) that consists of a PWM current source rectifier (CSR) and inverter (CSI) feeding an induction motor. The procedure includes dimensioning of the input and output filters, as well as the dc-link choke. State-of-the-art SGCT devices are employed in the design and their losses and junction temperatures are calculated. The converter design is made so that the switches in the inverter operate at their maximum specified junction temperature. An example design of a 4.16 kV, 1 MW drive is included. Losses of semiconductors and passive components are calculated for different operating points.**

I. Introduction

Medium-voltage power electronics is a field of continuously growing importance for a wide range of applications. Cycloconverters, as well as grid or load commutated converters applying conventional thyristors are used especially in applications with very high power demands which can not be met with state-of-the-art self-commutated converters at comparable prices. Today the majority of medium voltage converter and drive manufacturers offer PWM voltage source converters (VSC) in a power range from 300 kVA to 30 MVA.

An alternative to VSCs are current source converters (CSC), which employ inductors (chokes) instead of capacitors in the intermediate dc circuit. CSCs are available as medium voltage drives for high power industrial applications such as fans, pumps, compressors, mixers, and conveyors where a fast dynamic performance is not critical. The power ratings of CSCs vary between 100 kW and 7 MW for line voltages of 2.4 kV to 6.6 kV. Symmetrical Gate Commutated Thyristors (SGCT) are usually applied. They offer a bidirectional voltage blocking capability of 6.5 kV and an explosion-free converter design in case of device failures. CSCs feature a very low part count (high reliability and availability), simple and robust short circuit protection (dc-link choke), simple voltage scaling (SCGT series connection), balanced semiconductor loss and junction temperature distribution, integrated sine filter and inherent four-quadrant operation when used with an active front-end (AFE). Furthermore, operation without transformer between CSC and grid is possible. As main drawbacks, CSCs suffer from limited dynamic performance (large dc-link choke) and difficult parallel connection.

In the literature it is possible to find several publications about the structure, function and the design of components of CSCs. These include guidelines for designing the output filter [1], the input filter [2]–[5], and the dc-link choke [6], [7]. The selection of semiconductors, on the other hand, has not yet been properly discussed, though some work concerning loss calculation in SGCTs can be found in [8].

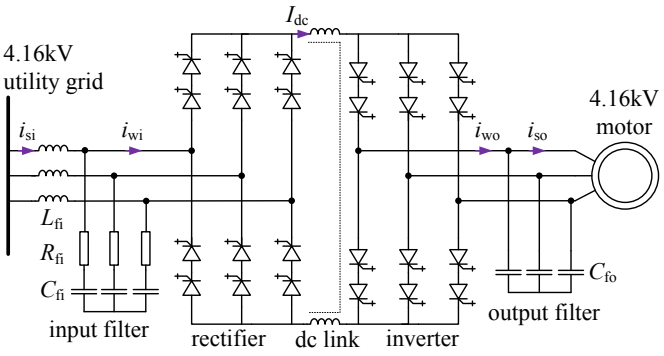


Fig. 1. Circuit configuration of current source converter

The goal of this paper is the introduction of a complete design procedure of passive and active elements for an exemplary 1 MW drive with AFE and IEEE-519 compliance. The power semiconductor dimensioning is done on the basis of a previously developed loss model which was applied to various VSC topologies [9]–[11]. The model was verified by direct junction temperature measurements with an infrared camera [12]. Finally, losses of semiconductors and passive components are considered for different operating points.

II. Structure and requirements of PWM-CSC

The converter being considered is shown in Fig. 1. It consists of input filter, PWM rectifier, dc current link, PWM inverter and output filter feeding a 4.16 kV induction machine. Both rectifier and inverter are pulse-width modulated on the basis of a scheme specially developed for CSCs. The input and output filters are necessary for the commutation process, as well as for the filtering of the converter currents. The rectifier together with the dc-link choke acts as a current source for the inverter. Requirements and design aspects of the converter being considered are listed in Table I.

III. Modulation

The pulse patterns of CSR and CSI should generally satisfy two conditions: (a) The dc current I_{dc} should be continuous, and (b) the inverter PWM current i_{wo} should be defined by

TABLE I
DATA FOR DESIGN OF CURRENT SOURCE CONVERTER

Modulation	CSR	SHE 5, 7, 11 + m_a $\rightarrow$ 800 Hz (8 pulses)
	CSI	SHE 5, 7, 11 and 13 $\rightarrow$ 900 Hz (9 pulses)
Line voltage	grid	4.16 kV
	motor	4.16 kV
Cooling system		water, double-sided
Max. junction temp.		125 °C
Water temp.		50 °C
Line harmonics		IEEE-519 compliant
Motor	power	1 MW
	load angle	27°
	eq. resistance	55 mΩ
	eq. inductance	4 mH
Semicond.	GCU04AA-130	6500 V 400 A
	GCU08BA-130	6500 V 800 A
	GCU15CA-130	6500 V 1500 A

I_{dc}. Both requirements can be summarized in one switching constraint: At any instant of time (excluding commutation intervals), there are only two sets of series-connected switches conducting, i.e. one on the top half of the bridge, and the other in the bottom half. [13], [14]

Several modulation techniques have been developed for CSCs, such as Trapezoidal Pulse Width Modulation (TPWM), Space Vector Modulation (SVM) and Selective Harmonic Elimination (SHE) (e.g. [3], [14]). The latter one was chosen for this work, since it provides a good harmonic spectrum at low switching frequencies for output frequencies higher than 21 Hz [15].

The inverter SHE pattern is tuned for eliminating harmonics of order 5, 7, 11 and 13. The rectifier SHE pattern eliminates only harmonics 5, 7 and 11, but enables the control of the modulation index $m_a = \hat{I}_{w,1}/I_{dc}$. This translates to a switching frequency of 900 Hz for the inverter and 800 Hz for the rectifier. These frequencies correspond to the ones observed in currents i_{wo} and i_{wi}, respectively. The switching frequency of each SGCT is only half of that frequency. Details of the modulation can be taken from [14].

A generic SHE pulse pattern for the elimination of two harmonics plus m_a control is depicted in Fig. 2. Depending on the harmonics to be eliminated, different angles θ_i are obtained when solving the associated equation system. For eliminating the 5th, 7th, 11th and 13th harmonic as configured in the inverter modulation, the resulting angles are 0°, 1.60°, 15.14° and 20.26°. The amplitude of the output current is controlled through the dc-link current magnitude, which can be adjusted by the rectifier modulation scheme, namely through modulation index m_a and the phase shift α adjustment. This enables also unity –or optimum– input power factor [14], [16]. For each modulation index m_a value, a different set of angles for the PWM pattern is obtained. A plot showing the SHE

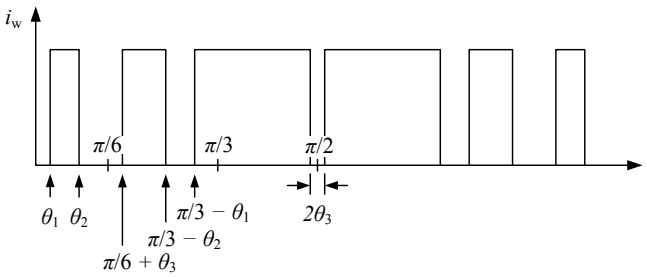


Fig. 2. Generic SHE 6-pulse pattern (half-cycle) with bypass pulse ($2\theta_3$) for the elimination of two harmonics and m_a control (for use in rectifiers) [14]

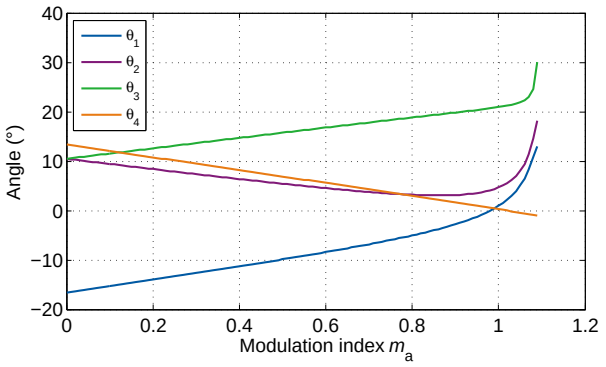


Fig. 3. SHE modulation angles for eliminating harmonics 5, 7 and 11 with variable m_a

angles used in the rectifier as a function of m_a is presented in Fig. 3. The maximum modulation index m_a is 1.09, higher values give no solution to the the equation system.

IV. CONVERTER DESIGN

The design flow of the CSC is shown in Fig. 4. Initially, an optimum output filter is selected. After that, inverter and load are simulated and the dc-link current I_{dc} is adjusted, so that the maximum junction temperature $T_{j,max}$ = 125 °C for a given SGCT is not exceeded. With this dc current I_{dc}, the input filter can be designed such that IEEE-519 recommendations are met. The passive elements design is completed by the dc-link choke selection, which limits the maximum dc current ripple. Thereafter, the entire converter with the designed components is simulated and the junction temperatures of the inverter switches are verified again. The specified junction temperature $T_{j,max}$, IEEE- 519 and ripple restrictions are compared to the simulation results. Once all conditions have been fulfilled, the junction temperatures of the rectifier switches are calculated. If these junction temperatures exceed the $T_{j,max}$ limit, the next larger current rating of the semiconductor should be selected until the junction temperature is below the limit in the worst-case operating point.

A. Output Filter

A current source inverter requires a three-phase filter capacitor C_{fo} at its output to allow the commutation of the switching

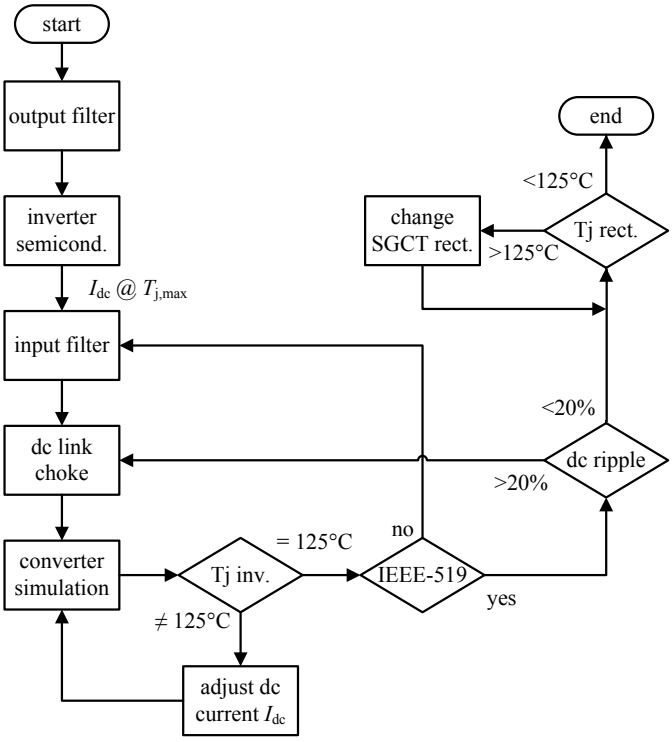


Fig. 4. Flow chart of CSC design procedure

semiconductors. The capacitors provide a current path for the energy stored in the load inductance. If not used, a high-voltage spike would be induced and the switches would be damaged. Another purpose of the capacitors is acting as output filter, smoothing the load voltage and current waveforms. According to [1], the output filter should:

1) Enable the lowest possible current rating of the inverter for a given motor
2) Maintain good control of torque and speed over the entire frequency range (avoid LC resonant modes)
3) Minimize the winding losses caused by current harmonics

These criteria lead to three restrictions that limit the capacitance value [1]:

$$C_{\text{fo}} < \frac{2I_{\text{so}} \sin\phi}{\omega_{\text{s,max}} V_{\text{so}}} \tag{1a}$$

$$C_{\text{fo}} < \frac{1}{\omega_{\text{s,max}}^2 L_{\text{m}}} \tag{1b}$$

$$C_{\text{fo}} > \frac{1 + I_{\text{wo},h}/I_{\text{so},h}}{h^2 \omega_{\text{s,min}}^2 L_{\text{ml}}} \tag{1c}$$

where

ϕ: load angle,
V_{so}: phase voltage in the load,
ω_{s}: output frequency,
L_{m}: magnetizing inductance of the motor and
L_{ml}: parallel connection of the magnetizing and leakage inductance.

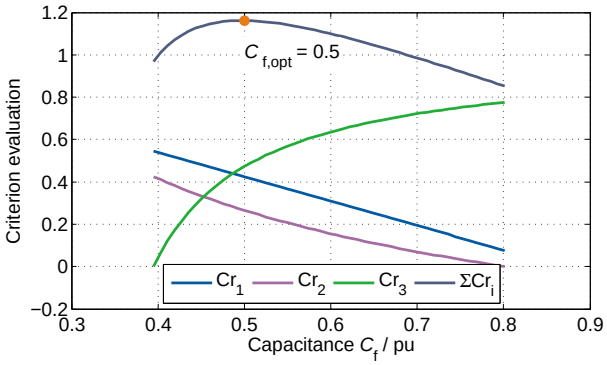


Fig. 5. Evaluation of criteria for finding an optimum output filter capacitance

The subscript h (in $I_{\text{wo},h}$, $I_{\text{so},h}$) represents the lowest harmonic present in the modulation. In (1a), rated values in pu are considered: $I_{\text{so}} = V_{\text{so}} = \omega_{\text{s,max}} = 1$ pu and $\phi = 27°$. In (1b), $\omega_{\text{s,max}} = 1$ pu and $L_{\text{m}} = 1.248$ pu. Eq. (1c) limits the lowest order current harmonic magnitude present in the load current. For the SHE modulation selected, $h = 17$ and $I_{\text{wo},17} = 0.106$ pu. $I_{\text{so},17}$ was limited to 0.25 pu at a frequency of 21 Hz, which is the minimum recommended for SHE modulation [15]; L_{ml} was set to 0.071 pu. These conditions result in an output filter capacitance in the range of

$$0.39 < C_{\text{fo}} < 0.80 \tag{2}$$

In order to find the optimum value between these boundaries, simulations for different C_{fo} values were carried out and each criteria was evaluated. For this purpose, three evaluation functions were implemented:

$$\text{Cr}_1 = \frac{|I_{C,\text{max}} - I_C(C_{\text{fo}})|}{I_{C,\text{max}}} \tag{3a}$$

$$\text{Cr}_2 = \frac{|\omega_{\text{s,max}} - \omega_{\text{r}}(C_{\text{fo}})|}{\omega_{\text{s,max}}} \tag{3b}$$

$$\text{Cr}_3 = \frac{|I_{\text{so},17,\text{max}} - I_{\text{so},17}(C_{\text{fo}})|}{I_{\text{so},17,\text{max}}} \tag{3c}$$

where $I_{C,\text{max}} = 2I_{\text{so}} \sin\phi$, $\omega_{\text{s,max}} = 1$ pu, $I_{\text{so},17,\text{max}} = 0.25$ pu and $\omega_{\text{r}} = 1/\sqrt{L_{\text{m}} C_{\text{fo}}}$. The higher the value of these functions, the better the capacitance value for that given criterion.

The optimum capacitance value is then given by

$$C_{\text{fo,opt}} = \max(\text{Cr}_1 + \text{Cr}_2 + \text{Cr}_3). \tag{4}$$

It equals $C_{\text{fo,opt}} = 0.5$ pu as the plot of Fig. 5 (ΣCr_i) shows. For the electric machine selected in the simulations (4.16 kV, 1 MW), this results in a capacitance of $C_{\text{fo}} = 92$ µF. It is important to note that the output filter is dependent on the load attached to it, and not to the maximum converter power output S_{C}.

B. Power Semiconductors

The power semiconductor design involves calculating conduction and switching losses. With these results and a thermal model, it is possible to calculate the junction temperature T_{j}

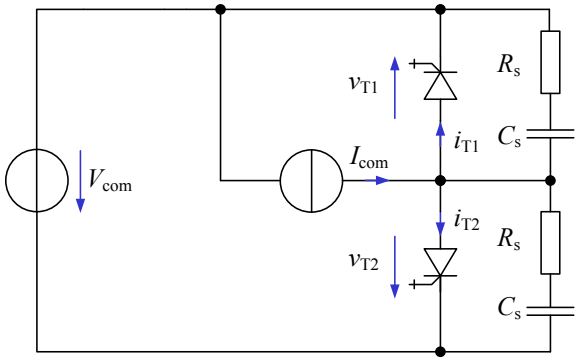


Fig. 6. Generic CSC commutation cell

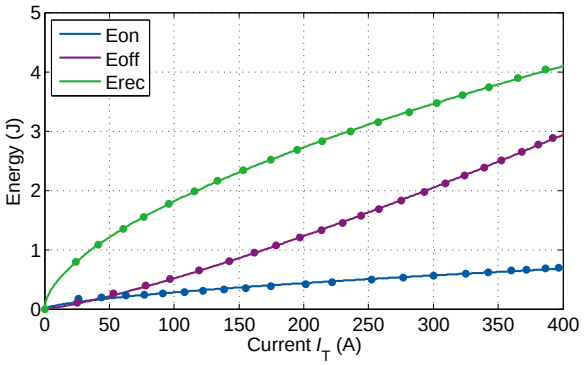


Fig. 7. Approximated switching losses for the SGCT GCU04AA-130

TABLE II
LOSSES IDENTIFICATION FOR NATURAL AND FORCED COMMUTATION

device voltage	switching	loss type on	off	rec	comm. type
$v_T > 0$	on	×			natural
	off		×		forced
$v_T < 0$	on				forced
	off			×	natural

and to determinate the maximum power output of the inverter, such that $T_j = T_{j,max}$.

1) Commutation Types: A classification of the commutation types and the corresponding switching losses is required for the calculation of the switching losses. An SGCT has three different types of switching losses: turn-on losses, turn-off losses and reverse recovery losses. A generic commutation cell for a CSC is shown in Fig. 6. There are natural and forced commutations. During natural commutation,

- T2 turns on from forward blocking voltage (turn-on losses)
- T1 turns off into reverse blocking voltage (reverse recovery losses).

For forced commutation,

- T2 turns off into forward blocking voltage (turn-off losses)
- T1 turns on from reverse blocking voltage (negligible losses).

In natural commutations, turn-on losses and reverse recovery losses are significant. In forced commutations, only turn-off losses have to be considered. Table II summarizes the occurring switching losses where v_T is the voltage across an SGCT [8]. The application of the conditions of Table II allows a simple assignment of switching losses to commutation events and power semiconductors by the observation of the device voltage polarity before and after commutations in converter simulations.

2) Semiconductor Loss Calculation: The method used for calculating semiconductor losses has been applied in previous publications (e.g. [9]–[11]) and was experimentally verified in [12]. Summarizing, conduction losses are calculated using an on-state voltage model derived from the datasheet and simulated voltage and current waveforms.

$$v_T(t) = A_{cond} i_T(t)^{B_{cond}} + C_{cond} \tag{5}$$

$$P_{cond} = \frac{1}{T_1} \int_0^{T_1} v_T(t) i_T(t) dt \tag{6}$$

where A_{cond}, B_{cond} and C_{cond} are the fitting constants for a given SGCT. For the switching losses, each commutation event $t_{sw,j}$ is identified and the corresponding losses are calculated, see Table II and (7).

$$E_{sw,x} = \frac{v_T(t_{sw,j})}{V_{ref}} (A_x i_T(t_{sw,j})^{B_x}) \tag{7}$$

where A_x and B_x are the fitting constants for each switching loss type (turn-on losses *on*, turn-off losses *off* and reverse recovery losses *rec*), calculated using datasheet energy plots. V_{ref} is the reference voltage for which the datasheet loss functions were measured. As an example, fitted loss functions for the SGCT GCU04AA are plotted in Fig. 7. Table III lists the fitting constants for the semiconductors being considered. An important characteristic of SGCTs, as seen in Fig. 7, are the relatively high reverse recovery losses. For a current of 200 A in SGCT GCU04AA-130, reverse recovery losses are 2.25 and 6 times higher than turn-off and turn-on losses, respectively.

3) Thermal Calculation: With the losses and the equivalent thermal circuit of Fig. 8 it is possible to estimate the junction temperature T_j. From the SGCT datasheet $R_{th,j\text{-}f}$ and $T_{j,max}$ are extracted. $R_{th,f\text{-}a}$ and T_a depend on the cooling system used. In this case, double-sided water cooling is considered with a maximum ambient temperature of $T_a = 50\,°C$. $R_{th,f\text{-}a}$ values for different semiconductor diameters are listed in Table IV.

4) Maximum Inverter Power: To estimate the maximum inverter power, the dc current I_{dc} is adjusted until the maximum admissible temperature $T_{j,max} = 125\,°C$ of the semiconductors is achieved, for a load angle of $\phi = 27°$. As switches, two series-connected SGCTs were considered. Table V shows the results for the three currently available SGCTs. The configura-

TABLE III
CURVE-FITTING CONSTANTS FOR SGCT LOSS CALCULATION

	GCU04AA	GCU08BA	GCU15CA
A_{on}	0.014584943	0.014390788	0.163929993
B_{on}	0.641230755	0.629180923	0.316384002
A_{off}	0.001581005	0.001976866	0.001952963
B_{off}	1.256327984	1.186264250	1.179357281
A_{rec}	0.121709455	0.112243519	0.204390308
B_{rec}	0.586844510	0.612589123	0.538369831
A_{cond}	0.117750910	0.098667340	0.124004376
B_{cond}	0.650192964	0.618398666	0.539414813
C_{cond}	1.606343990	1.344610567	1.413399276

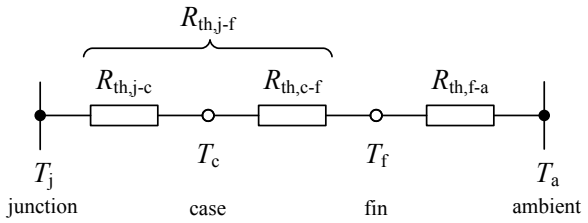


Fig. 8. Thermal equivalent circuit for T_{j}-calculation

TABLE IV
THERMAL RESISTANCE VALUES FOR DOUBLE-SIDED WATER COOLING

SGCT	Diameter (mm)	Th. resistance (K/W) $R_{\text{th,j-f}}$	$R_{\text{th,f-a}}$
GCU04AA-130	38	0.04	0.03
GCU08BA-130	47	0.025	0.0195
GCU15CA-130	63	0.014	0.0109

TABLE V
MAXIMUM INVERTER POWER

SGCT	I_{dc} (A)	$I_{\text{s,out}}$ (A)	S_{C} (MVA)
GCU04AA-130	**210**	**173**	**1.25**
GCU08BA-130	334	268	1.95
GCU15CA-130	541	422	3.06

tion that uses the SGCT GCU04AA-130 is selected for further calculations, since the converter power of S_{C} = 1.25 MVA (1.11 MW) is the closest to the motor power used as load.

C. Input Filter

The design algorithm for the RLC filter is depicted in Fig. 9. As input, the resonance frequency f_{r} of the filter is required. This value, along with the condition of unity power factor and the desired attenuation of the filter at f_{r} determine the initial values of the filter components L_{fi}, C_{fi} and R_{fi}. A simulation of the circuit using these values is carried out to verify the IEEE-519 restrictions [17]. If the harmonic content does not exceed the limits, the results are stored and a new resonant frequency f_{r} is selected. If the limits are exceeded, filter inductance and

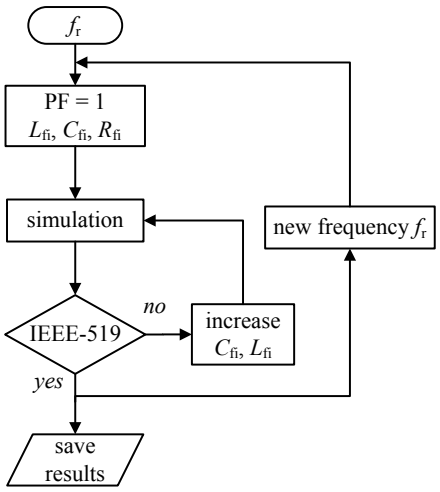


Fig. 9. Input filter design diagram

capacitance are increased until the restrictions are met. The second part of the algorithm –not shown in the diagram– involves computing the filter power for each configuration. The minimum power configuration is selected as the optimum filter.

The resonant frequency should be selected, such that

$$f_{\text{r}} = \frac{1}{2\pi\sqrt{C_{\text{fi}}L_{\text{fi}}}} < \frac{f_h}{2} \tag{8}$$

where f_h represents the frequency of the lowest order generated harmonic [4]. For the modulation scheme used, h = 13.

In [2], an expression for the displacement angle $\theta = \angle V_{\text{si}} - \angle I_{\text{si}}$ is given,

$$\theta = \tan^{-1}\frac{V_C}{I_{\text{dc}}X_C} - \tan^{-1}\frac{I_{\text{dc}}X_L}{V_C\left(1-\dfrac{X_L}{X_C}\right)} \tag{9}$$

where V_C stands for the voltage across the input capacitor.

Combining (8) and (9) and setting θ = 0 (power factor PF = 1) and V_C = 1 pu,

$$\tan^{-1}\frac{C_{\text{fi}}}{I_{\text{dc}}} - \tan^{-1}\frac{I_{\text{dc}}}{C_{\text{fi}}(f_{\text{r}}^2-1)} = 0 \tag{10}$$

with all variables in pu. Using (10) and (8) it is possible to find C_{fi} and L_{fi}. R_{fi} can be found by selecting the filter gain at the resonant frequency,

$$\left|\frac{i_{\text{si}}}{i_{\text{wi}}}\right| = \sqrt{1+\frac{1}{(\omega_{\text{r}}C_{\text{f}}R_{\text{f}})^2}} \tag{11}$$

As suggested in [2], filter gain $|i_{\text{si}}/i_{\text{wi}}|$ should lie between 4 and 7.

With the equations described above, a filter combination can be found for any given input resonance f_{r} with PF = 1 as a condition. However, this procedure does not ensure IEEE-519 compliance [17]. Thus, each filter combination is simulated and optimized until IEEE-519 restrictions are met. Finally, the

TABLE VI
CHARACTERISTIC DATA OF CSC DESIGN

$V_{\text{ll,in}} = V_{\text{ll,out}}$	4.16 kV	L_{fi}	11 mH
S_{C}	1.29 MVA	C_{fi}	90 µF
ϕ	27°	R_{fi}	2.4 Ω
$I_{\text{dc,max}}$	219 A	L_{dc}	26 mH
$I_{\text{so,max}}$	179 A	C_{fo}	92 µF
$T_{\text{j,rect}}$	109 °C	SGCT rect	GCU08BA-130
$T_{\text{j,inv}}$	124 °C	SGCT inv	GCU04AA-130

combination of minimum power is selected. The power of the input filter S_{fi} is calculated as follows

$$S_{\text{fi}} = \sum_{h=1}^{\infty} \left(h I_{\text{s},h}^2 X_L + \frac{h V_{C,h}^2}{X_C} \right) \tag{12}$$

D. Dc-link Choke

The purpose of the dc-link inductor is to ensure a dc current with a low ripple. Normally, the ripple is limited to r = 20%. The current ripple is caused by the harmonic content of the rectifier output voltage v_{ro} and the impedance of the dc-link:

$$\sum_{h=1}^{\infty} \frac{V_{\text{ro},h}}{2\pi f_h L_{\text{dc}} + R_{\text{dc}}} = r I_{\text{dc}} \tag{13}$$

where $V_{\text{ro},h}$ is the amplitude of the h-th voltage harmonic of rectifier ouput voltage and f_h its frequency. R_{dc} is the internal resistance of the choke and it can be neglected, since

$$R_{\text{dc}} \ll 2\pi f_h L_{\text{dc}} \tag{14}$$

for the frequencies f_h present in the voltage spectrum. This allows the calculation of the L_{dc} value on the basis of the rectifier output voltage waveform,

$$L_{\text{dc}} = \frac{1}{2\pi r I_{\text{dc}}} \sum_{h=1}^{\infty} \frac{V_{\text{ro},h}}{f_h}. \tag{15}$$

E. Final Converter Design

Once the converter components have been designed, an adjustment of the parameters is realized using a simulation of the complete converter, see Fig. 4. All the requirements, such as semiconductor junction temperature of the inverter, IEEE-519 compliance and dc current ripple are verified. Fig. 10 shows the line current i_{si} and its harmonic spectrum, indicating the IEEE-519 limits. It can be appreciated, that the filter was design complies with the standard requirements.

Finally, the semiconductor junction temperatures T_{j} of the rectifier are calculated. For $T_{\text{j}} > 125\,°\text{C}$, which is the case for this system, an SGCT with a higher current rating must be selected until $T_{\text{j}} < 125\,°\text{C}$. Thus, it is ensured that the inverter is operated at full capacity. The final CSC design is shown in Table VI.

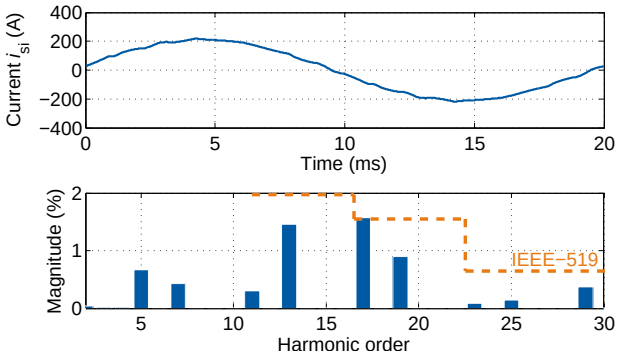


Fig. 10. Line current i_{si} and its harmonic spectrum with IEEE-519 limits ($V_{\text{ll,out}}$ = $V_{\text{ll,in}}$ = 4.16 kV, S_{C} = 1.29 MVA, I_{dc} = 219 A, I_{so} = 179 A, ϕ = 27°)

V. CONVERTER LOSSES

A. Semiconductor Losses

The semiconductor losses are calculated using (6), (7) and the fitting constants listed in Table III, as explained in section IV-B2.

B. Input Filter and Dc-link Choke

According to [8] it is possible to estimate the inductor losses using the formula

$$P_L = 0.67 \times 0.45\% \times \left(\frac{L}{0.12\,\text{pu}} \right)^{0.75} \tag{16}$$

where L is a 3-phase inductance in pu system. The formula is based on the losses of a sine filter inductance of 0.12 pu in a 3L-NPC VSC (copper and iron). The factor 0.67 is a scaling factor for currents with no substantial low-order harmonics.

For input filter losses in L_{fi},

$$P_{L\text{fi}} = 0.67 \cdot 0.45\% \cdot \left(\frac{0.26}{0.12\,\text{pu}} \right)^{0.75} = 0.0053\,\text{pu} \tag{17}$$

and for dc-link choke L_{dc},

$$P_{L\text{dc}} = 2 \cdot 0.67 \cdot 0.45\% \cdot \left(\frac{0.59/2}{3 \cdot 0.12\,\text{pu}} \right)^{0.75} = 0.0052\,\text{pu} \tag{18}$$

C. SGCT Snubber

An SGCT snubber was not included in section IV, since it is recommended to use the configuration proposed in the datasheet. The snubber comprises a conventional RC circuit connected in parallel to the SGCT. Since SGCTs enable high rates of current rise (e.g. di/dt = 1 kA/µs) the stray inductance of the stack is sufficient to limit the rate of current change.

Significant snubber losses occur in the resistance of the RC snubber. In a conventional RC circuit, where the capacitor C is charged and discharged, the energy dissipated in the resistor R equals

$$E_R = CV^2 \tag{19}$$

TABLE VII
OPERATION POINTS FOR DIFFERENT TORQUE VALUES

M (pu)	I_{so} (A)	ϕ (°)	I_{dc} (A)
0.2	42	47	65
0.4	67	32	90
0.6	96	27	122
0.8	127	26	157
1.0	160	27	195

However, for the RC circuit in the commutation network shown in Fig. 6 the losses in the resistor R_s for a charge-discharge cycle are not always determined just by the voltage and capacitance values. Through an analysis of the commutation cell, the following expression can be found:

$$E_{Rs} = \begin{cases} C_s V_{com}^2 & \text{if} \quad (R_s I_{com})^2 \geq 8V_{com}^2 \\ C_s \left(V_{com}^2 - \dfrac{(R_s I_{com})^2}{8} \right) & \text{if} \quad (R_s I_{com})^2 < 8V_{com}^2 \end{cases} \tag{20}$$

where the influence of the commutation current I_{com} is important under certain conditions. For the snubber loss calculation, V_{com} is replaced by the SGCT voltage after the SGCT turn-off and I_{com} by the SGCT current before the turn-off.

D. Results

The loss distribution, efficiency and junction temperatures for different operating points (different torques at constant converter voltage and output frequency) are shown in Fig. 11. Tab. VII shows the details of each simulated operation point.

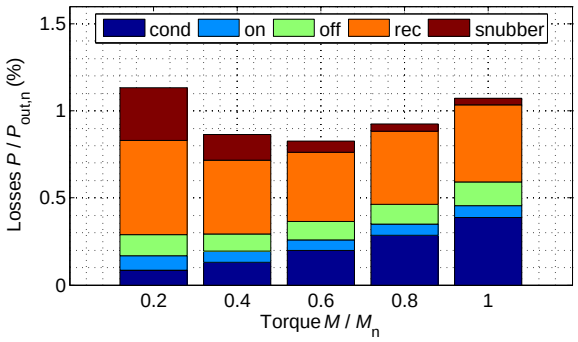
The reverse recovery losses clearly dominate the switching losses of the symmetrical IGCTs (Fig. 11a, Fig. 7). Furthermore, it is interesting to note that for $M/M_n \geq 0.4$ the inverter efficiency is $\eta \geq 0.98$ considering the semiconductor losses only. The rectifier and inverter loss distribution for the nominal operating point (torque M = 1 pu), as well as the total converter losses are shown in Fig. 12. Semiconductor and snubber losses cause about 70% of the converter losses.

As seen in Fig. 12, the losses in the rectifier are higher than in the inverter, even though the switching frequency of each device is lower (400 Hz at the rectifier vs. 450 Hz at the inverter). This can be explained through Fig. 13: The current and voltage stress of the semiconductors during commutation is higher in the rectifier than in the inverter.

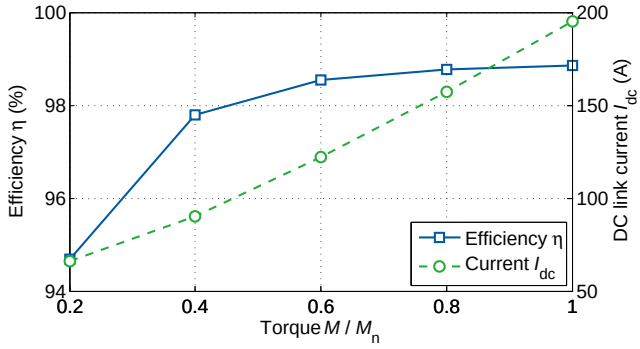
The 3-phase damping resistor R_{fi} of the input filter, which was selected to achieve a filter gain $|i_{si}/i_{wi}|$ of 7 at the resonant frequency f_r, as suggested in [2] and discussed in [5], was not considered in the loss calculation. It adds 8.63% additional converter losses at nominal load, which would make such a design undesireable. A reconsideration of the dimensioning criterion is advisable in future work.

VI. CONCLUSIONS

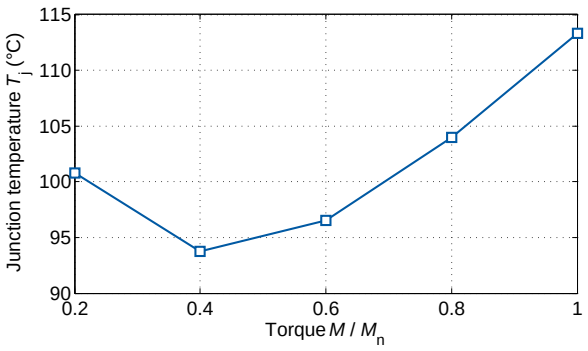
A complete current source converter design procedure was presented. Passive and active elements were dimensioned according to the requirements of the drive and the grid. The converter switches and output power were determined, such that the SGCTs in the inverter operate at their maximum junction temperature. Furthermore, the loss distribution of semiconductors and snubbers in the inverter was considered Finally the losses of rectifier, dc current link and inverter are derived for nominal operation.



(a)



(b)



(c)

Fig. 11. Inverter semiconductor losses (a), efficiency and dc-link current (b) and junction temperature (c) for different torque conditions including snubber effect ($V_{ll,out}$ = $V_{ll,in}$ = 4.16 kV, $P_{out,n}$ = 1 MW, SGCT GCU04AA-130)

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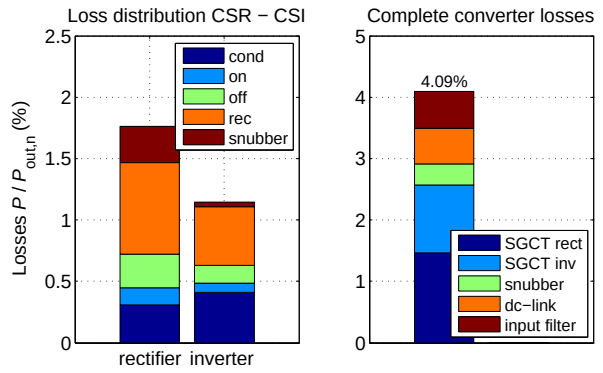

Fig. 12. Rectifier and inverter loss distribution and total converter losses for torque $M = 1\,\text{pu}$ ($V_{\text{ll,out}} = V_{\text{ll,in}} = 4.16\,\text{kV}$, $P_{\text{out}} = 1\,\text{MW}$, $I_{\text{dc}} = 195\,\text{A}$, $I_{\text{so}} = 160\,\text{A}$, $\phi = 27°$, SGCT inverter GCU04AA-130 at $T_{\text{j}} = 113\,°\text{C}$, SGCT rectifier GCU08BA-130 at $T_{\text{j}} = 103\,°\text{C}$)

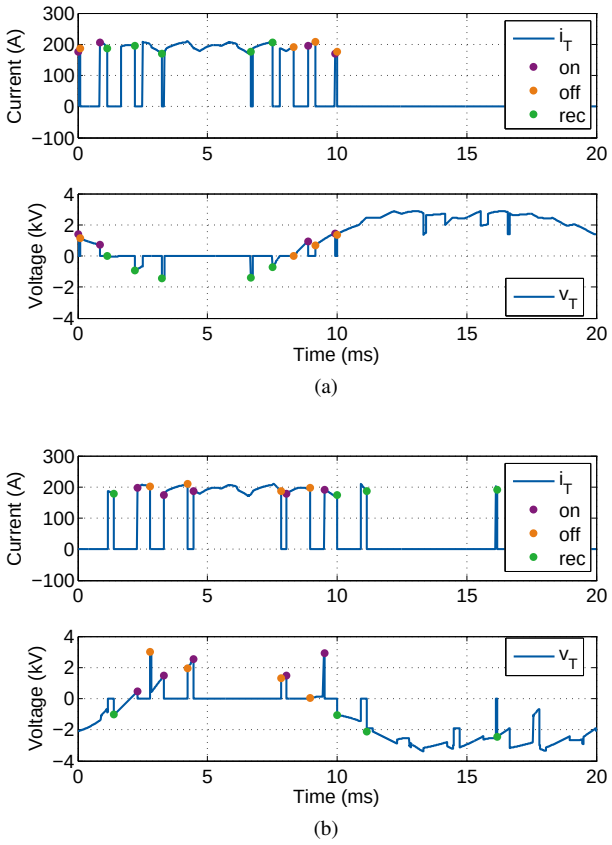

Fig. 13. SGCT current and voltage waveforms for rectifier (a) and inverter (b) for torque $M = 1\,\text{pu}$, including commutation type identification ($V_{\text{ll,out}} = V_{\text{ll,in}} = 4.16\,\text{kV}$, $P_{\text{out}} = 1\,\text{MW}$, $I_{\text{dc}} = 195\,\text{A}$, $I_{\text{so}} = 160\,\text{A}$, $\phi = 27°$)

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