Investigation of oscillations in a 6.5-kV, 1-kA SiC diode module

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Keywords

<<Silicon Carbide (SiC)>>, <<Diode>>, <<Noise>>, <<Simulation>>

Abstract

SiC technology is attractive for power devices, as it potentially offers many advantages over traditional Si-based devices. However, many issues still need to be properly addressed in order to become a popular and cost-effective alternative to Si devices. One of these issues are high-frequency oscillations that appear during commutation, which limit the switching speed of the device and can produce undesired EMC problems. This paper analyzes the source of the oscillations that appear during the turn-off transient of a recently developed SiC PiN diode module (6.5 kV, 1 kA). A behavioral model derived from the device characterization was elaborated and verified. Through simulation, the main ringing sources are identified and assessed. The positive effect of an RC snubber circuit for dampening the oscillations is presented and experimentally verified.

Introduction

Parasitic oscillations during the switching transients may cause EMC problems in the gate driver or device failure due to high voltage spikes. For the machine, high dv/dt and common mode voltages may lead to windings' isolation and bearing failures [1–3]. With SiC devices and their faster switching rates this issue becomes critical for their application and will have an effect on the device performance. Some investigations about this subject have been recently reported, mainly related to low-voltage low-current devices [4–9]. In these cases, the oscillations are mainly caused by high current change rates di/dt and the use of unipolar devices without tail current. As a consequence, circuit parasitics such as stray inductances and capacitances start to resonate.

The device here analyzed is a 6.5-kV 1-kA SiC PiN diode module, whose characterization was presented in [10]. During the diode turn-off transient, oscillations in the range of 4.5 to 6.5 MHz are present, as seen in Fig. 1. As stated in [2, 11], there are four possible sources to this behavior:

1. High di/dt during commutation
2. High di/dt after the reverse recovery current peak
3. Duration of the reverse recovery process (resonant frequency)
4. Unequal current distribution in the paralleled dies inside the module

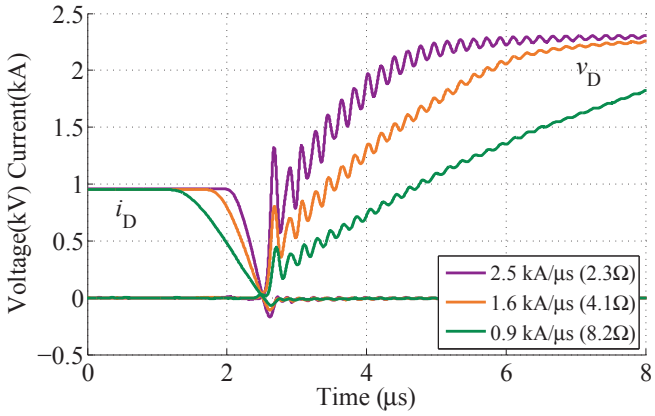


Figure 1: Oscillations during the diode turn-off transient for different di/dt (IGBT gate turn-on resistance) values (2.4 kV, 1 kA, 25°C, di/dt = 0.9...2.5 kA/µs)

Since these oscillations appear at common di/dt ratings for Si devices – i.e. 0.9...2.5 kA/us at 1 kA, 2.4 kV, see Fig. 1 – where usually no ringing is observed, the first source can be discarded. The fourth source can also be discarded by observing the shape of the reverse recovery current in the SiC diode (just one reverse recovery peak). Only the second and third sources remain as possible sources. To investigate them, a simulation of the switching transient using behavioral models of the IGBT and the SiC diode was developed. The interactions of the circuit parasitics with the oscillations was also investigated.

The following procedure was used to determine the different factors that affect the oscillations: First, the parasitic elements in the test circuit were extracted out of measurements. As a second step, a behavioral model of the IGBT and diode were elaborated and validated through measurements. With the validated models, the different parameters involved in the oscillations were analyzed through simulation. Out of this analysis, possible solutions and their limitations were derived. An RC snubber circuit showed good results dampening the oscillations. This alternative was simulated and experimentally verified in the test bench.

Test bench and parameter extraction

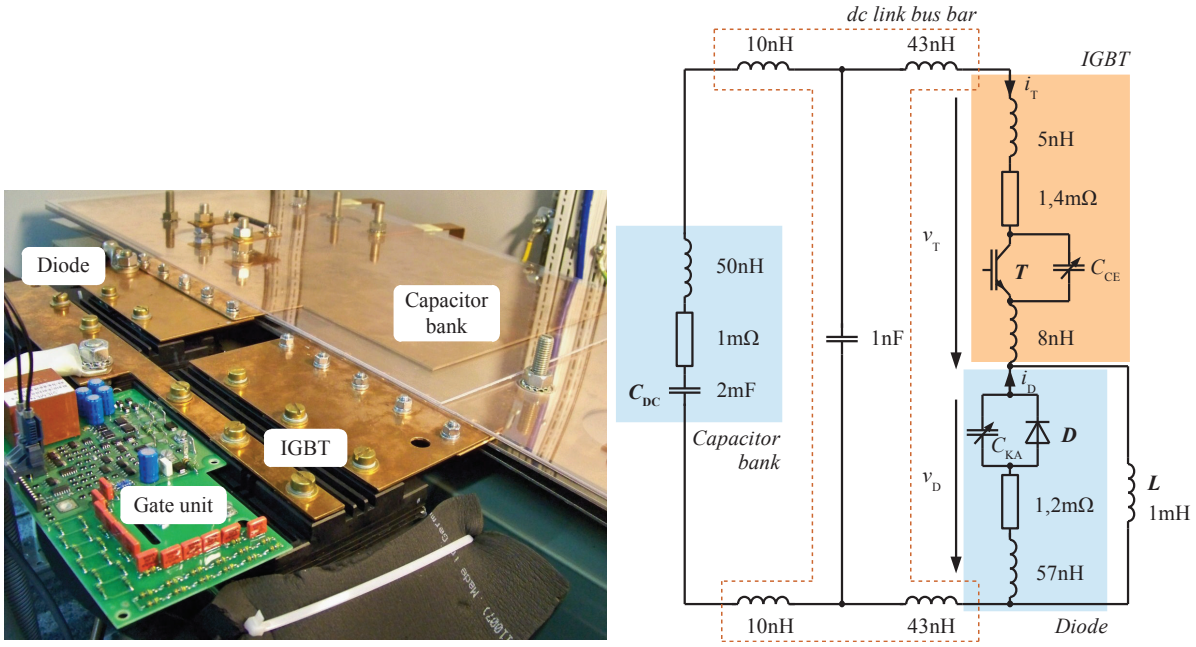
The test bench used to characterize the switching behavior of the diode is a buck converter, as shown in Fig. 2. The diagram can be divided in four elements: dc-link capacitor (including ESR and ESL taken from the data sheet), dc busbar and the diode and IGBT (FZ600R65KF2) modules.

The SiC diode module prototype is packaged in a standard industrial device housing of $140 \times 130\,\mathrm{mm}^2$. Inside the module there are 4 DCB, each with 20 SiC diode chips. Connected in parallel they achieve a current rating of 1000 A (80 chips) per module. The maximal blocking voltage is 6.5 kV. Each chip has an active area of $7.1\,\mathrm{mm}^2$, totalizing $5.68\,\mathrm{cm}^2$ per module. This module was characterized in [10]; for details about the diode technology used, refer to [12].

The dc busbar was modeled as an array of stray inductors for the positive and negative bus connected through a stray capacitance due to the laminated design. The capacitance was calculated out of the geometry assuming ideal parallel plates and the inductance was estimated through measurements and computer calculations based on the Partial Element Equivalent Circuit (PEEC) method with the software InCa3D.

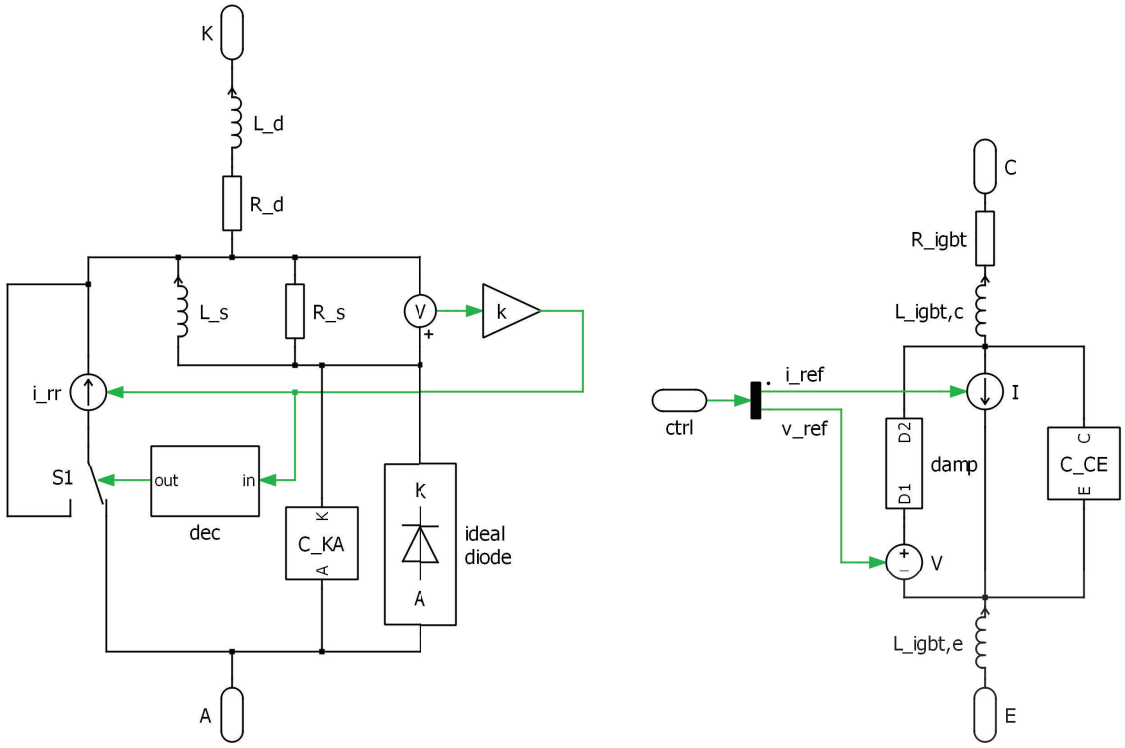
The diode and IGBT parasitic elements considered were the module inductance, junction capacitance and on-state resistance. The IGBT and diode modules' internal stray inductance was calculated by applying the basic equation $v = L \cdot \mathrm{d}i/\mathrm{d}t$ to measured waveforms during the device commutation.

The voltage-dependent junction capacitance C_j was determined by connecting a high-ohmic resistor (1 MΩ) to the device terminals and using the discharge curve corresponding to $C_\mathrm{j}R$ to extract the capacitance value for different voltage levels. This is a simple method, but due to the voltage dependency of C_j does not deliver accurate results. Nonetheless, these were good enough to be used as an initial guess for the simulation. The on-state resistance was approximated linearly from the on-state characteristic. The values for the extracted parameters are included in Fig. 2b.



(a) (b)

Figure 2: Test bench photo (a) and equivalent circuit with extracted parameters (b)



(a) Diode model [13] (b) IGBT model

Figure 3: Semiconductor models as used in PLECS simulation software

Device modeling and validation

The device models as implemented in the simulation software PLECS are presented in Fig. 3. To study the oscillations, the diode model is able to produce a reverse recovery current peak and shape that can be adjusted by the user, see Fig. 3a. The model includes the parasitic values of *L*, *R* and *C* mentioned above.

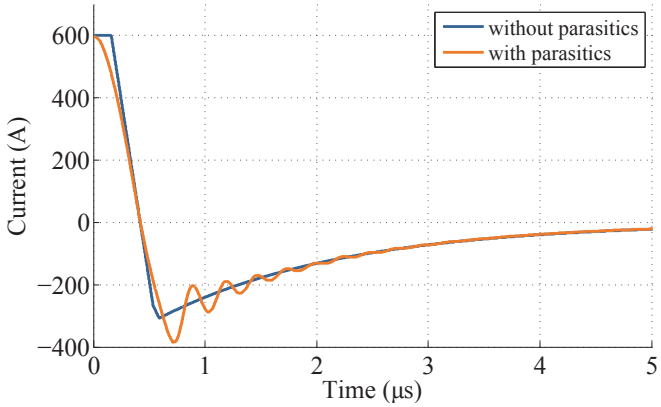
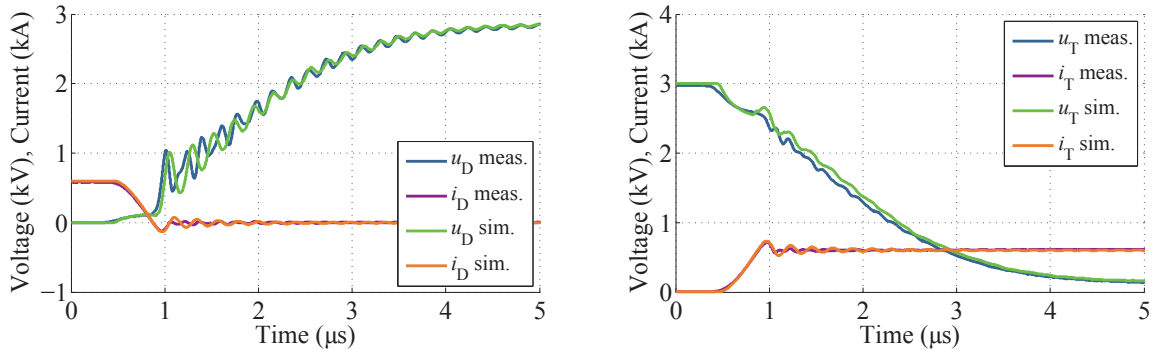


Figure 4: Comparison of the simulated reverse recovery current waveform with and without the effect of circuit parasitics



(a) Diode turn-off (b) IGBT turn-on

Figure 5: Comparison measurement/simulation at calibration point (V_{dc} = 3 kV, I_L = 600 A, ϑ_j = 25°C, $R_{g,on}$ = 4.1 Ω)

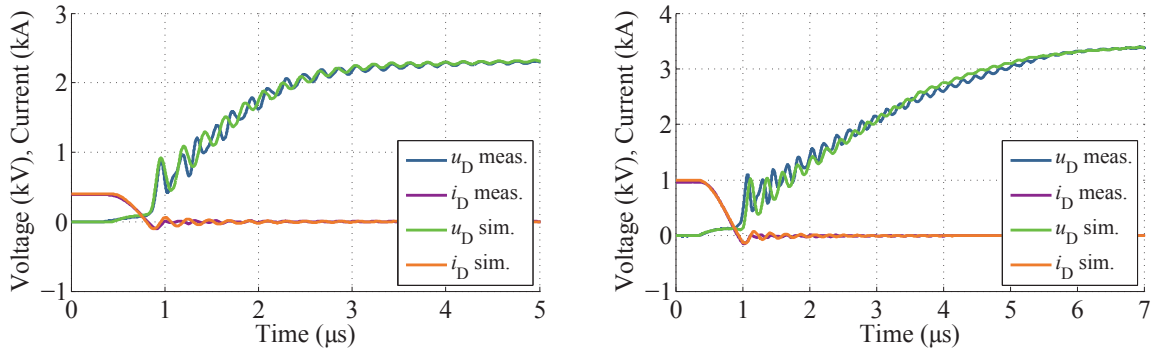
For the realization of a reverse current peak, the model proposed in [13] was adapted: a combination of `L_s`, `R_s` and the decoupling block `dec` together with the current source `i_rr` and an ideal diode are used to generate a reverse recovery current with an adjustable shape, by choosing the reverse recovery peak I_{rrm} and the current change rate after the peak di_{rr}/dt. The current waveform obtained through the simulation is the result of the input parameters defined by the user in the diode model and the superimposed oscillations of the circuit parasitics, as shown in Fig. 4.

The IGBT model has as input the desired dv/dt and di/dt values. These input values together with a reference waveform are given to the IGBT to generate the desired waveforms. Under the block `damp` a damping resistor was modeled. This element acts as a current-controlled resistor which is calibrated by measurement data. Additionally, values for the internal inductance, resistance and capacitance can be entered.

The information needed by the model – e.g. the data for the block `damp` – is taken from a reference measurement. This is shown in Fig. 5, with both simulated and measured waveforms. In order to validate the model, the input variables for the simulation, such as dc-link voltage V_{dc} or current change rate di/dt ($R_{g,on}$) were varied and the simulation results were compared to the measurements, see Figs. 6 and 7.

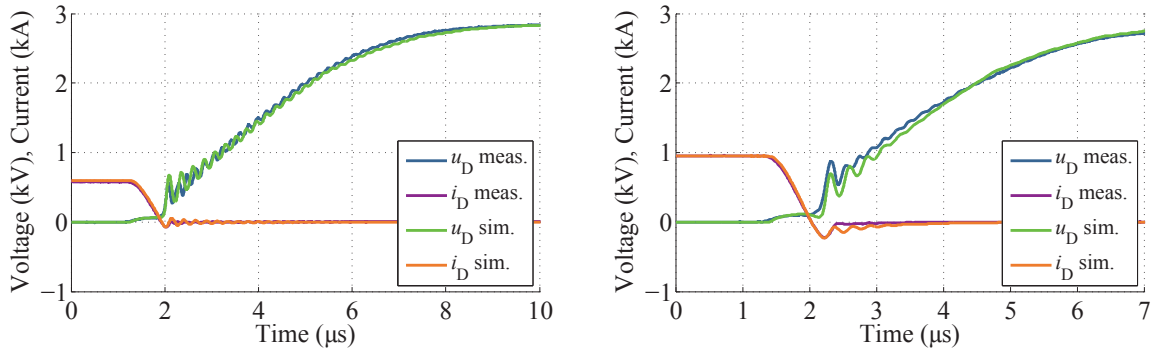
It can be appreciated that the frequency of the oscillations in the simulation could be matched accurately only for the last part of the turn-off transient. In the measured waveforms the oscillation frequency is not constant, but the result of the superposition of two oscillations with variable frequencies that reach a final common frequency after a few microseconds. In the simulation model a constant frequency was modeled and was matched with the final part of the oscillation, see Figs. 5-7.

In the Fig. 7b an interesting behavior can be observed. At high junction temperature (ϑ_j = 125°C) the voltage oscillations in the SiC diode almost completely disappear. Adjusting the shape of the reverse



(a) V_{dc} = 2.4 kV, I_L = 600 A (b) V_{dc} = 3.6 kV, I_L = 1 kA

Figure 6: Comparison measurement/simulation of the diode turn-off transient at different V_{dc} values (ϑ_j = 25°C, $R_{g,on}$ = 4.1 Ω)



(a) $R_{g,on}$ = 8.2 Ω, I_L = 600 A (b) ϑ_j = 125°C, I_L = 1 kA

Figure 7: Comparison measurement/simulation of the diode turn-off transient at a different $R_{g,on}$ and junction temperature ϑ_j (V_{dc} = 3 kV)

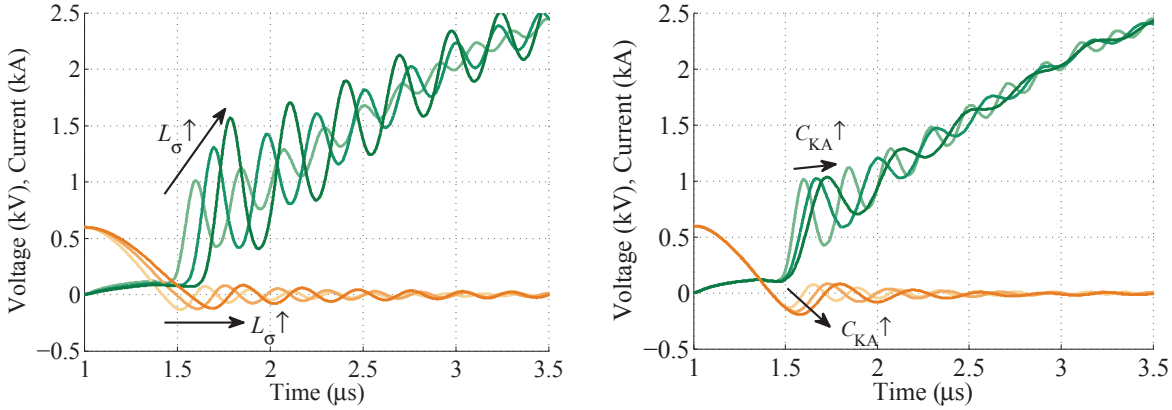
recovery current waveform in the simulation to the shape of the current at ϑ_j = 125°C delivered similar results. This indicates the reverse recovery shape has a direct influence in the parasitic oscillations. The next section uses the simulation models to study these effects.

Despite the drawbacks mentioned above, the model is able to generate waveforms that can be used to qualitatively assess the influence of the different parameters in the voltage oscillations during the diode turn-off, which is the main purpose of this investigation.

Simulative analysis

First of all, the most influential parameters were identified. As Fig. 2b shows, the largest parasitic inductance corresponds to the dc-link busbar, which dominates during commutation and has a direct effect on oscillations. Variation of the IGBT's junction capacitance and bus bar capacitance did not bring any major change and were left at their initial values. The diode's junction capacitance and the shape of the reverse recovery current, on the other side, are critical for the high-frequency oscillations and were given more attention.

In the first part of the analysis, the influence of the stray inductance in the commutation cirtcuit and the diode's junction capacitance is analyzed. A simulation of the turn-off transient of the SiC diode under different stray inductance values for the dc busbar connection was carried out, see Fig. 8a. It is clear that a low-inductive mechanical design is highly important. Stray inductance has to be kept as low as possible. However, there are certain limits given by the operating voltage of the devices and the required creepage distances and air gaps that have to be taken into account for the mechanical design. The selection of the



(a) Stray inductance L_σ = 106, 212, 318 nH (increase) (b) Diode's junction capacitance $C_{KA} = 1\ldots3C_{KA,ref}$

Figure 8: Influence of stray inductance inductance (a) and capacitance (b) in the oscillations, green: voltage, orange: current (V_{dc} = 3 kV, I_L = 600 A, $R_{g,on}$ = 4.1 Ω, ϑ_j = 25°C)

dc-link capacitors plays also an important role, low-ESL capacitors should be preferred.

As expected, a higher junction capacitance of the diode would reduce the frequency of the voltage ringing, see Fig. 8b. Here, the measured junction capacitance $C_{KA,ref}$ was increased threefold. A higher reverse recovery peak can be observed, due to the higher charge that needs to be evacuated from the base of the device. Regarding the voltage oscillation amplitude, no relevant change can be observed.

After analyzing the effect of inducances and capacitances in the oscillations, the influence of the reverse recovery waveform shape was studied. The reverse recovery behavior of a diode is related to its internal structure, as defined in the design phase of the semiconductor. For the diodes here analyzed this is described in [12]. With the behavioral model of the diode the shape of the reverse recovery current can be changed, without the need of changing variables in a physical model.

The first scenario, depicted in Fig. 9a, aims at assessing the influence of the reverse recovery current duration, without changing the di/dt before as well as after the current peak [2]. The simulations show a slight decrease in the amplitude as well as the frequency of the voltage oscillations. Changing the shape of the reverse recovery current as shown in Fig. 9a has a direct consequence in increasing the stored charge and, hence, the switching losses.

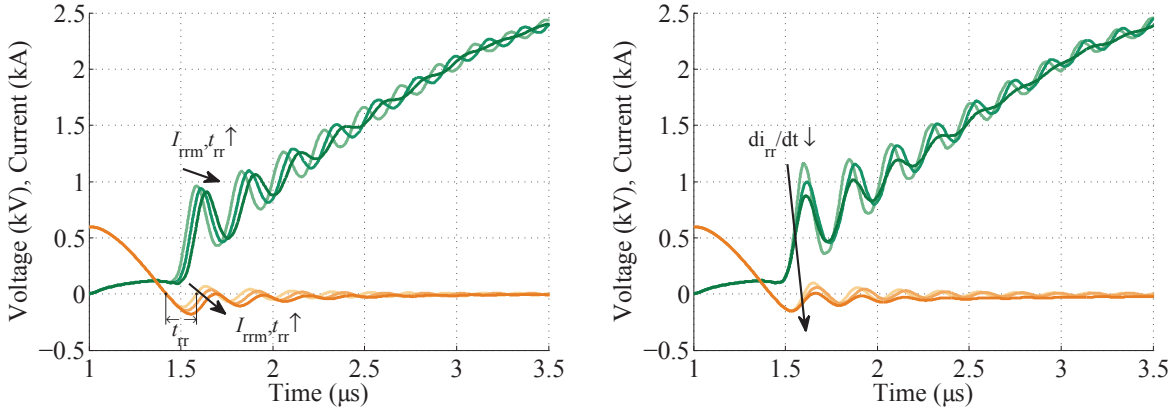
The current change rate after the reverse recovery current peak di_{rr}/dt is a critical parameter in diodes. For Si-devices, diodes labeled as *soft-recovery diodes* are popular, because they ensure a low di_{rr}/dt without snappy behavior. Oscillations caused by snappy diodes with a very high di_{rr}/dt and can lead to device failure [14]. Since the di_{rr}/dt increases with faster current switching speed di/dt the first voltage spike will also increase, see Fig. 1. This is a limiting factor for the switching speed and maximum device overvoltage. The simulation results in Fig. 9b indicate that a slower di_{rr}/dt is the best way to tackle the problem of the oscillations, as both current and voltage oscillations are reduced. Since the turn-off losses of this diode are under 100 mJ at 3 kV, higher losses can be accepted with a minimal impact on overall performance. As an example, considering a continuous current of 600 A in the full SiC diode module, the conduction loss P_{cond} dissipated equals to

$$P_{cond} = v_D i_D = 3.8\,\mathrm{V} \times 600\,\mathrm{A} = 2.3\,\mathrm{kW}. \tag{1}$$

If the diode commutates at a frequency of 800 Hz, switching losses amount to only 80 W, which is a negligible quantity. However, this solution translates into a redesign of the diode, which is not an option for the application designer and it is also constrained by the physical properties of the semiconductor materials.

A common solution for reducing parasitic oscillations in a circuit is the use of an RC snubber in parallel with the device that oscillates, see Fig. 10. To find the RC combination following method was used:

Considering that the stray inductance of the commutation circuit L_σ = 226 nH (see Fig. 2) and the frequency of the oscillations f_r lies between 4.5 and 6.5 MHz, the capacitance of the SiC diode C_{KA} can be



(a) I_{rrm} = 116, 147, 179 A, t_{rr} = 163, 203, 267 ns (b) di$_{rr}$/dt = 3.3. . . 1.9 kA/µs (decrease)

Figure 9: Influence of the simultaneous variation of reverse recovery current peak I_{rrm} and duration t_{rr} (a) and variation of the current change rate after the reverse recovery peak di$_{rr}$/dt (b) in the oscillations, green: voltage, orange: current (V_{dc} = 3 kV, I_L = 600 A, $R_{g,on}$ = 4.1 Ω, ϑ_j = 25°C)

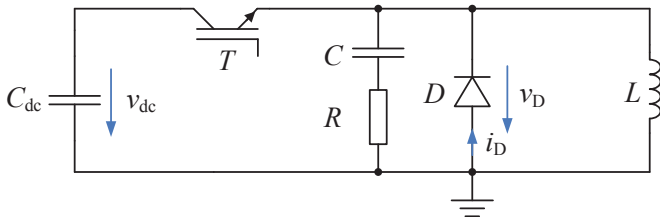


Figure 10: Test bench with an RC snubber added to the diode

estimates as follows:

$$C_{KA} = \frac{1}{(2\pi f_r)^2 L_\sigma}. \tag{2}$$

According to (2), C_{KA} has a value between 2.6 and 5.5 nF. The resistance R is determined by

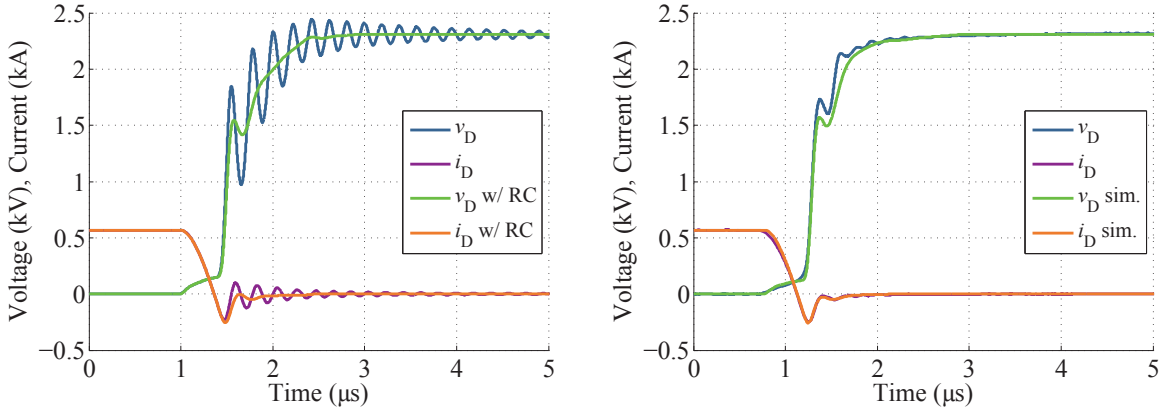
$$R = \frac{1}{2\xi}\sqrt{\frac{L_\sigma}{C_{KA}}} \tag{3}$$

and for critical damping (ξ = 1), it should be around 3.2 and 4.6 Ω. An initial value of C can be found by setting the cut-off frequency of the RC circuit to the frequency of the oscillations f_r, that is,

$$f_c = \frac{1}{2\pi RC} = f_r \tag{4}$$

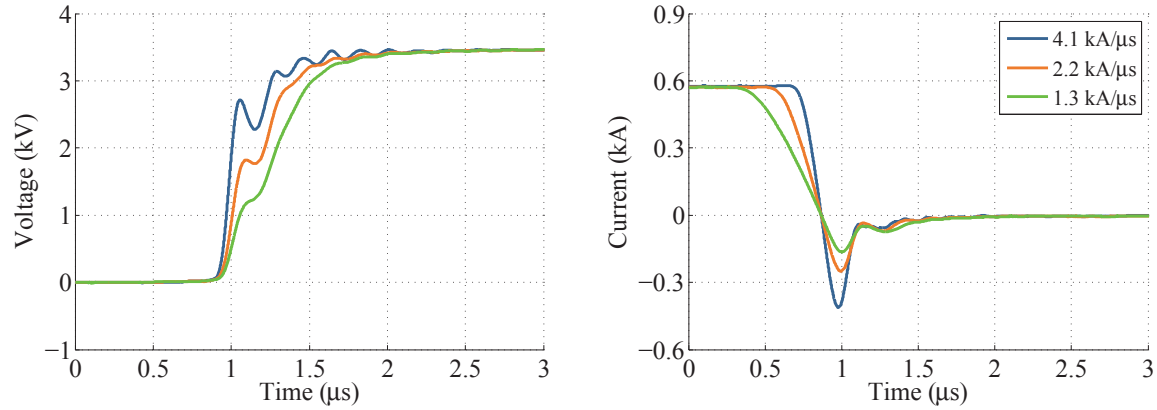
The values obtained for C are between 5.6 and 11.7 nF. Since 4.7 nF capacitors with 6 kV blocking voltage are a standard product, following combinations were experimentally tried out: C = 4.7, 9.4 nF; R = 3.3, 4.7 Ω.

An RC circuit of 9.4 nF, 4.7 Ω showed good results, as the simulations and measurements in Fig. 11 demonstrate. For the case of very high di/dt (4.1 kA/µs) the capacitance was increased to 14,1 nF. Slight differences between the simulated and measured voltages can be seen in Fig. 11b, because the IGBT was switched with a different gate unit than the one used before. With this RC snubber it was possible to switch on the IGBT at a higher di/dt without being limited by the overvoltages caused by the oscillations, see Fig. 12 for measurement results. Even with a threefold increase in the switching speed the oscillations are almost completely dampened by the RC snubber. Higher di/dts are also possible, as long as no overvoltages endanger the device; eventual oscillations can be dampened by readjusting the snubber circuit.



(a) Simulation with and without RC snubber (b) Comparison simulation and measurement

Figure 11: Effect of an RC snubber circuit connected to the diode ($C = 9.4\,\text{nF}$, $R = 4.7\,\Omega$, $V_{dc} = 2.3\,\text{kV}$, $I_D = 600\,\text{A}$, di/dt = 2.2 kA/µs)



(a) (b)

Figure 12: Measured voltage and current waveforms for diode turn-off at different di/dt with an RC snubber: $C = 9.4\,\text{nF}$, $R = 4.7\,\Omega$ for di/dt = 1.3, 2.2 kAµs; $C = 14.1\,\text{nF}$, $R = 4.7\,\Omega$ for di/dt = 4.1 kAµs ($V_{dc} = 3.5\,\text{kV}$, $I_D = 600\,\text{A}$, $\vartheta_j = 25°\text{C}$)

Regarding the extra losses added by the snubber circuit, these are comparable to the turn-off losses of the SiC diode. For one charge and discharge cycle of capacitor C at a voltage V, the energy E_C is given by

$$E_C = CV^2. \tag{5}$$

For $V = 3\,\text{kV}$ and $C = 10\,\text{nF}$, $E_C = 90\,\text{mJ}$. This value is low and, considering switching frequencies under 1 kHz, only a marginal addition to the overall converter losses, see Eq. (1)

Conclusions

The analysis of the oscillations during the turn-off transient of a newly introduced 6.5-kV 1-kA SiC PiN diode was presented. For this purpose, a behavioral model of the semiconductors involved was developed. A characterization of the test circuit used in the measurements was also necessary in order to model the phenomenon. The methodology used to develop the model and extract the circuit parameters was explained.

From the simulation results more insight into the sources of the oscillations was gained. The reverse

recovery current change rate di_{rr}/dt was identified as the main source for the oscillations. The stray inductance of the commutation circuit plays a major role in amplifying these oscillations; these demands a careful mechanical design of the power circuit, as well as the use of low-inductive components.

The diode could profit from a softer turn-off, reducing this way the oscillations during the commutation. Extra-losses have to be accepted as a drawback, which is not so critical, since SiC devices switching losses contribute only marginally to the overall device losses. However, this requires a redesign on die-level and, thus, it is not an alternative for application designers in the short term. From the application point of view, an RC snubber is an effective solution to this problem. The measurements confirmed that a value of 9.4 nF, 4.7 Ω achieves good results reducing the oscillations for this diode.

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