The hyperlink to the video stream in this virtual lecture is marked by the Video Campus Sachsen Logo.
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select TU-Dresden in the selection mask and than logon with the same ID and password as you use for OPAL or ZIH. Now the link guides you to the video stream.

Module SCT

Wrap-Up for preparation of the exam

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here 

"SCT_Module_Wrap.X.SS21"
1:31:23

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Outline of SCT1

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Lecture Semiconductor Technology I,
Prof. Dr. J. W. Bartha

Content

Outline of SCT1

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Lecture Semiconductor Technology I,
Prof. Dr. J. W. Bartha

Content

Outline

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behavior
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

Thank you very much for your attention!

All the very best for the upcomming exams!

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Relaxing vaccation!

»Wissen schafft Brücken.«