Zentrum für Hochleistungsrechnen

Invitation

for

ZHR-Kolloquium

Title: **Enhanced Floating Point for Multimedia on PC's: Standards and Engineering**

Referent: **Prof. Dr. David W. Matula,**
Department of Computer Science and School of Engineering and Applied Science,
Southern Methodist University, Dallas

Abstract:

Popular multimedia applications such as 3D graphics in computer games benefit from floating point units that are faster than those for scientific computing but require less precision. Multimedia applications typically exhibit small vector parallelism such as 4 components for 3D graphics transforms and 8 components for the MPEG IDCT providing opportunities for SIMD speedup. Announced enhanced x86 chips from AMD and Cyrix include paired single precision floating point in a double word. Intel's still privileged MMX 2 design

emphasizes 128 bit formats, suggesting possibly 4 component single precision SIMD floating point. Pipelined single cycle throughput single precision SIMD floating point is attainable for add and multiply at 300+ MHz, but essential divide and square root operations are bottlenecks with their current typical 20+ cycle iterative implementations.

The evolving solution is to provide hardware reciprocal and root reciprocal functions. The design challenge is to provide the increased speed in reciprocal and root reciprocal computation without sacrificing the spirit of the IEEE floating point standard that has proven so beneficial to applications in scientific computing. This presentation deals first with the properties of ulp accuracy, monotonicity, and ulp accurate differences that should serve as a standard for these sensitive low precision reciprocal functions. We then demonstrate why enhanced linear interpolation is more efficient than Newton Raphson refinement in computing reciprocal functions with these properties.

Location: **Willers-Bau, A 120**
Time: **Monday, May the 18th in 1998, 3.00 p.m.**

gez. Prof. Dr. W.E. Nagel