

Zentrum für Informationsdienste und Hochleistungsrechnen

EINLADUNG zum

ZIH - KOLLOQUIUM

Title: Patterns of inefficient performance behavior in GPGPU programs

Referent: Dominic Eschweiler Forschungszentrum Jülich

Abstract:

Writing efficient software for heterogeneous architectures equipped with modern accelerator devices presents a serious challenge to programmer productivity, creating a need for powerful performance-analysis tools to adequately support the software development process. However, such tools are rare and often still in an early design stage. To guide the design of such tools, we describe typical patterns of inefficient runtime behavior that may adversely affect the performance of applications that use general-purpose processors along with GPU devices through a CUDA compute engine. To evaluate the potential impact of these patterns on application performance, we further present a microbenchmark suite that allows the performance penalty of each pattern to be quantified with results obtained on an NVIDIA Tesla card indeed demonstrating significant delays. Based on these experiences, we formulate requirements of future performance tools for host-device ensembles.

Ort: Willers-Bau C 207 Zellescher Weg 12 - 14, 01069 Dresden

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gez. Prof. Dr. Wolfgang E. Nagel